


Switching Innovations

Virtual Espresso Webinar

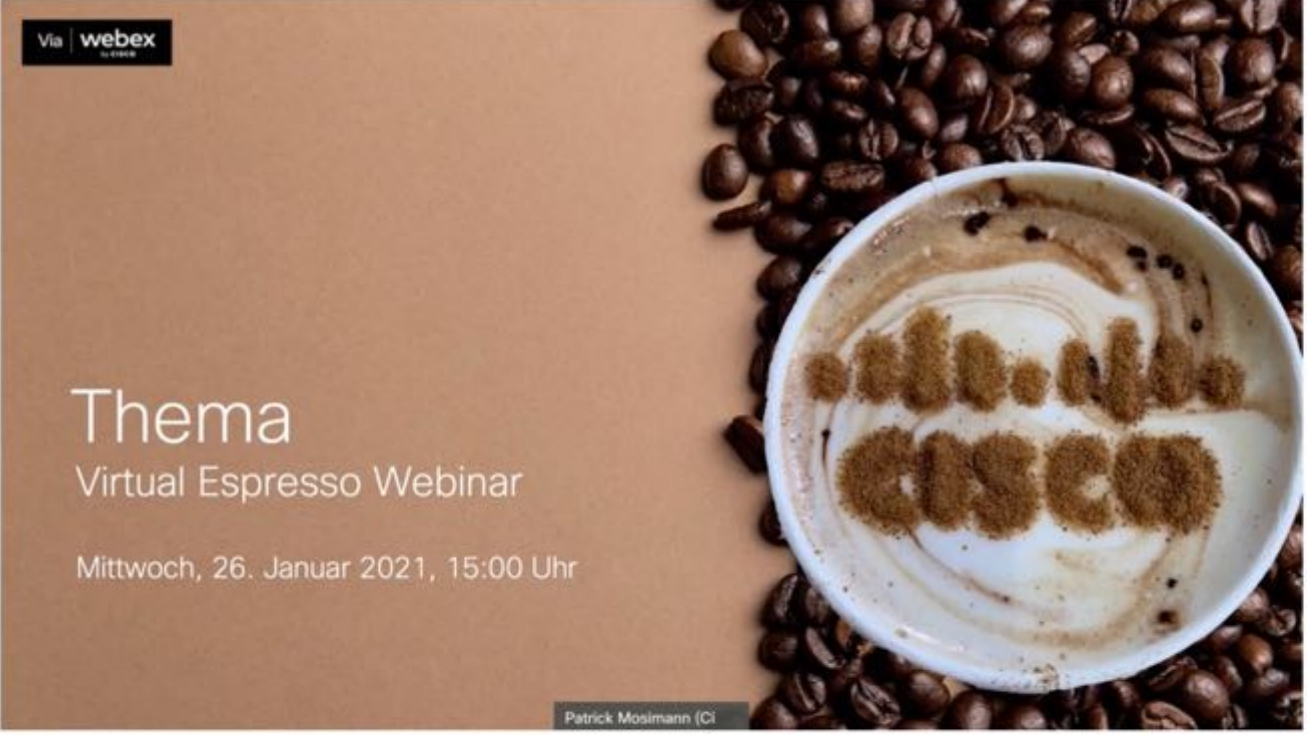
Mittwoch, 9. März 2022, 15:00 Uhr



👉 please utilise the Q&A function to get your question answered



Video




Patrick Mosimann (CI)

Ereignisdetails

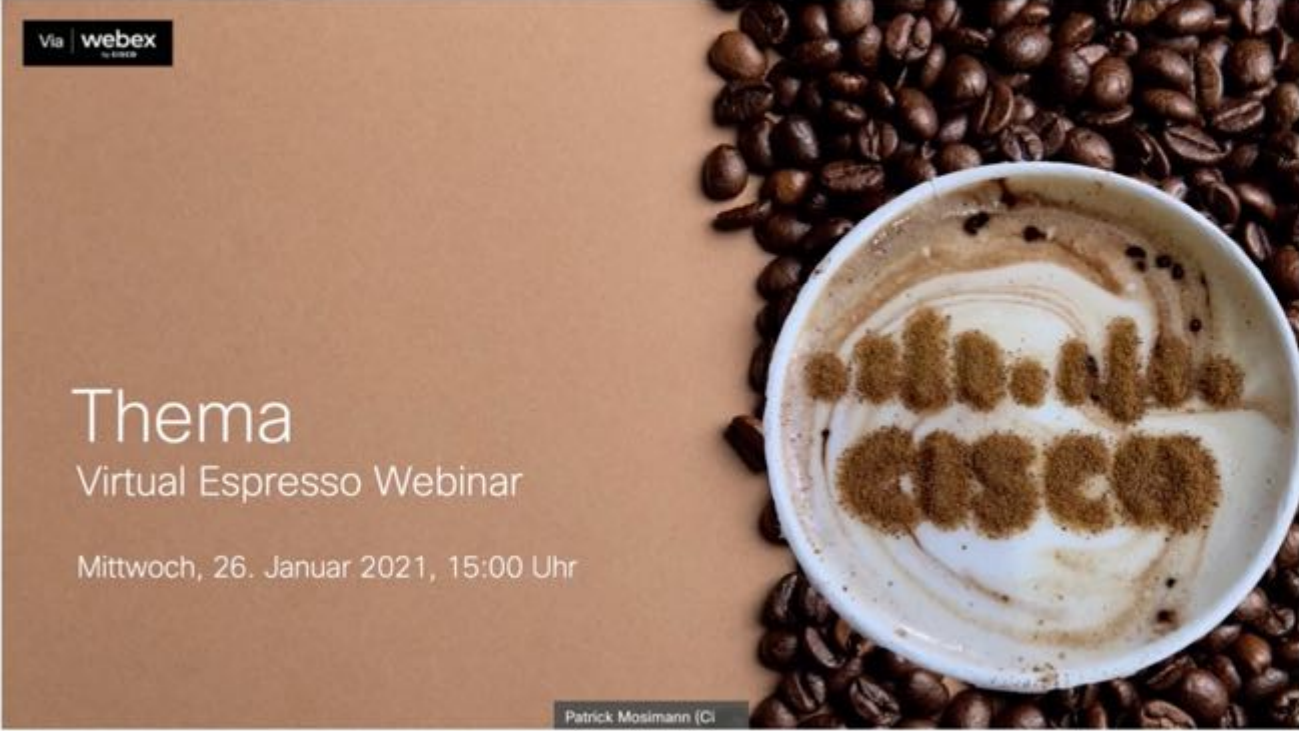
Virtual Espresso: Thema
25. Jan. 2022 21:30 -- 25. Jan. 2022 22:00
Moderator: Patrick Mosimann

Fragen & Antworten

👉 please utilise the Q&A function to get your question answered



Video



Via **webex** by CISCO

Thema

Virtual Espresso Webinar

Mittwoch, 26. Januar 2021, 15:00 Uhr

Patrick Mosimann (CI)

Fragen & Antworten

Meine Fragen (0) Gruppenfragen (0)

[Absenden](#)

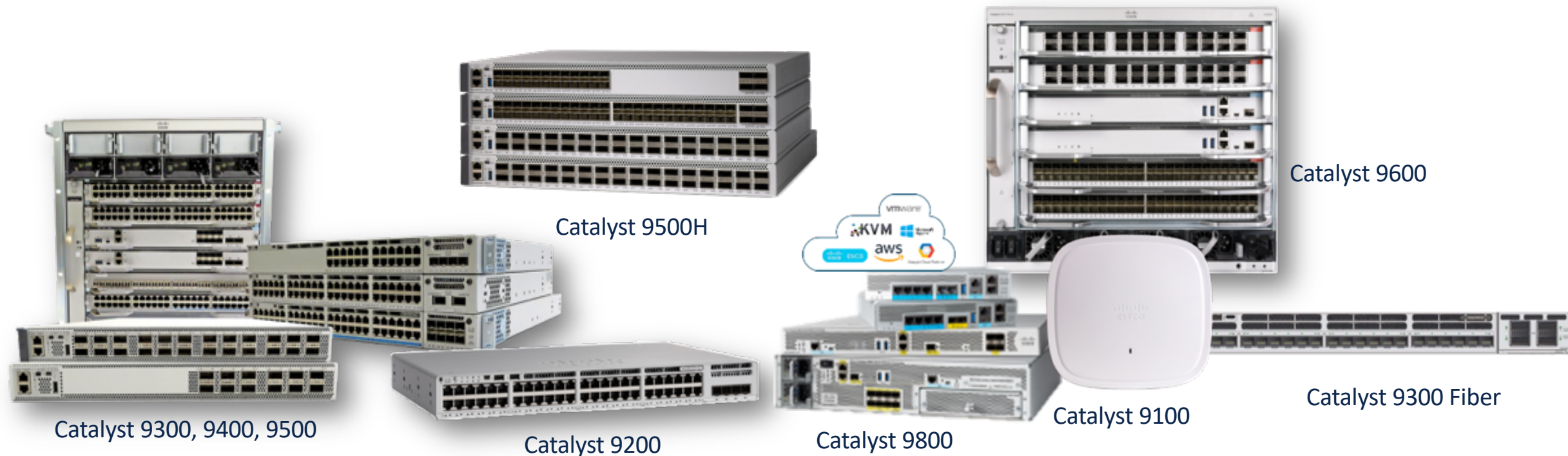
Von Ihnen gestellte Fragen sind hier aufgelistet.

?



Catalyst Full-Stack Switching overview

Corinne Rümmeli, Technical Solutions Specialist
Patrick Mosimann, Technical Solutions Architect
9. März 2022



Catalyst 9500H

Catalyst 9600

Catalyst 9300, 9400, 9500

Catalyst 9200

Catalyst 9800

Catalyst 9100

Catalyst 9300 Fiber

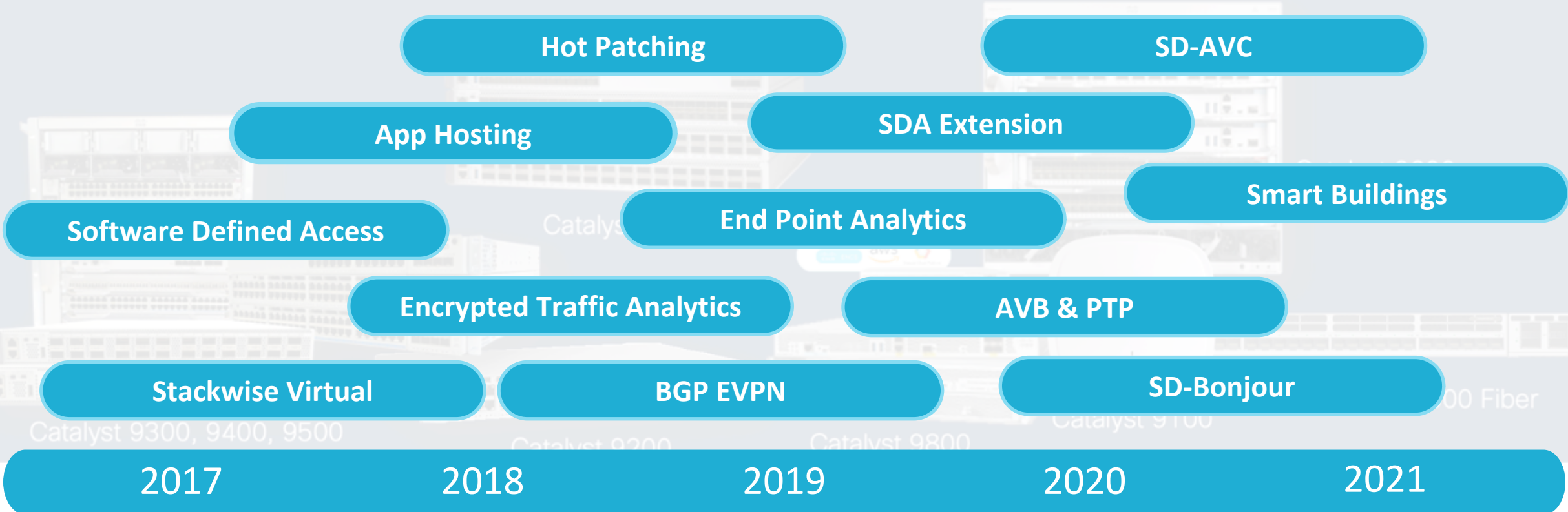
2017

2018

2019

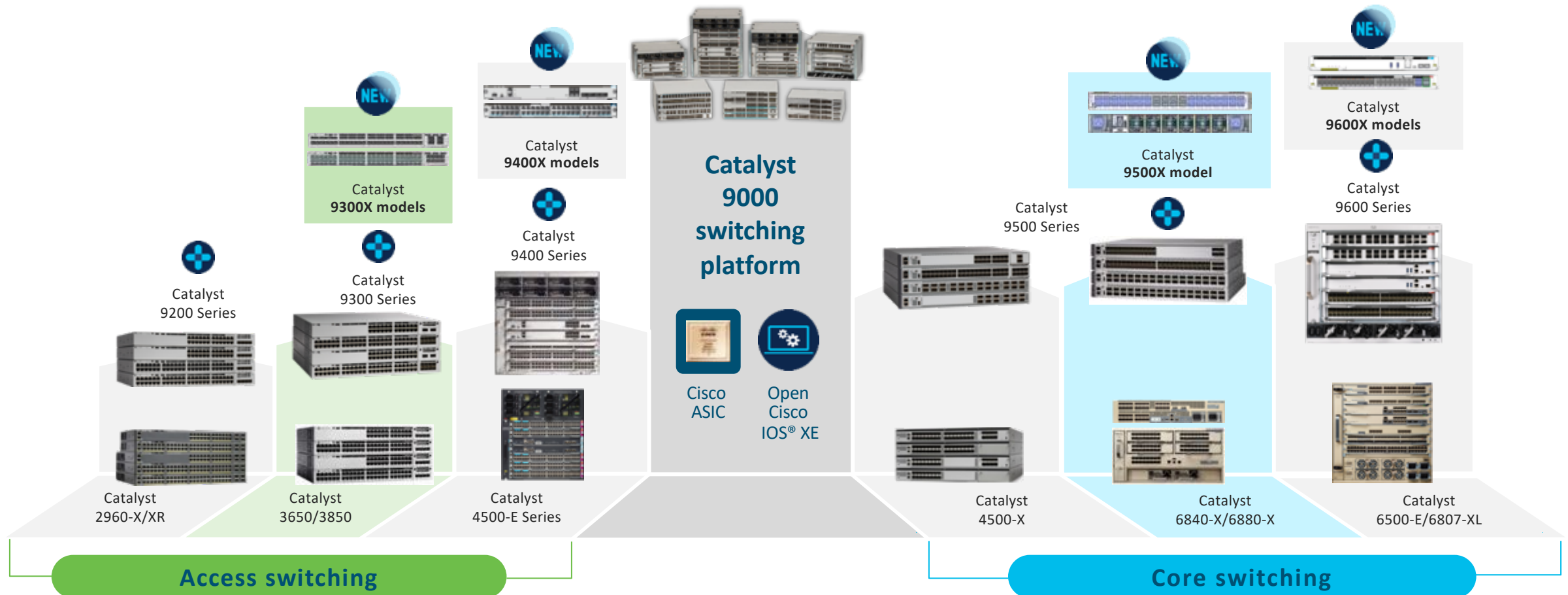
2020

2021



Catalyst 9000X – Expanding industry leadership

Adding the “X factor” to the industry’s leading switching family



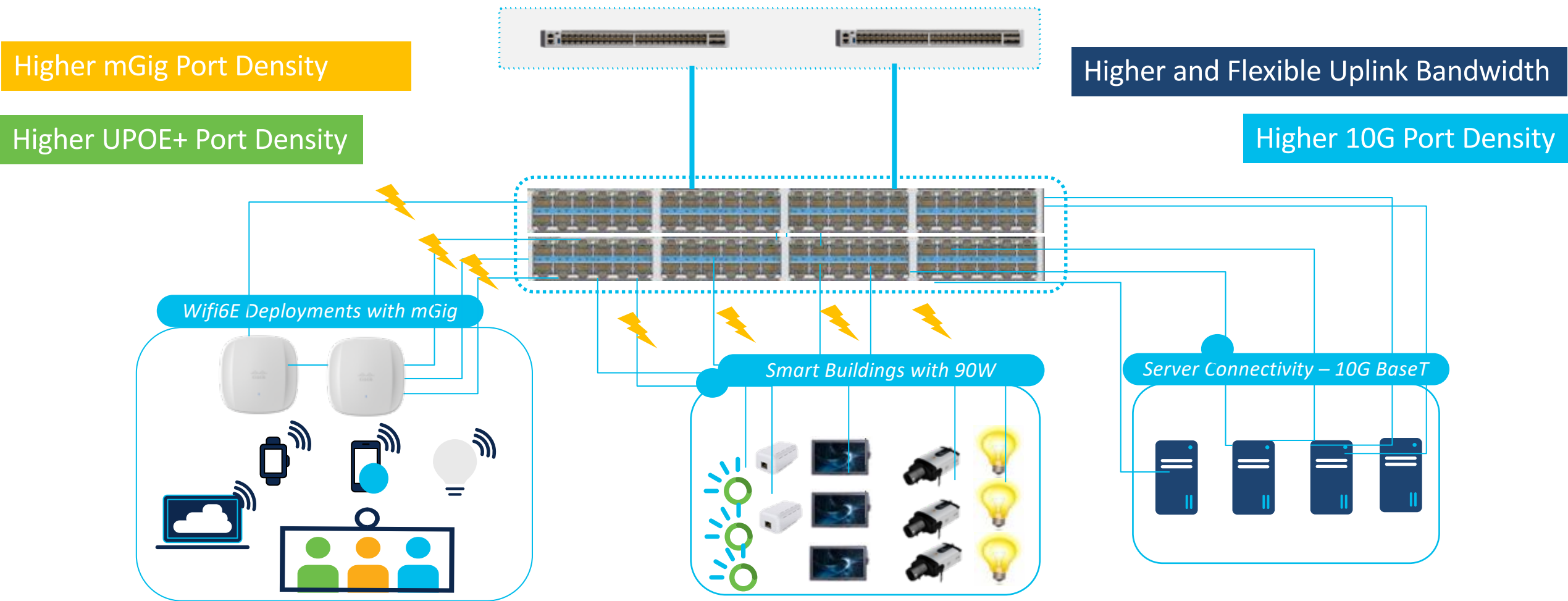
Agenda

- Access:
 - C9300-X
 - C9400-X
- Distribution/Core
 - C9500-X
 - C9600-X

Access



Enterprise Access Trends

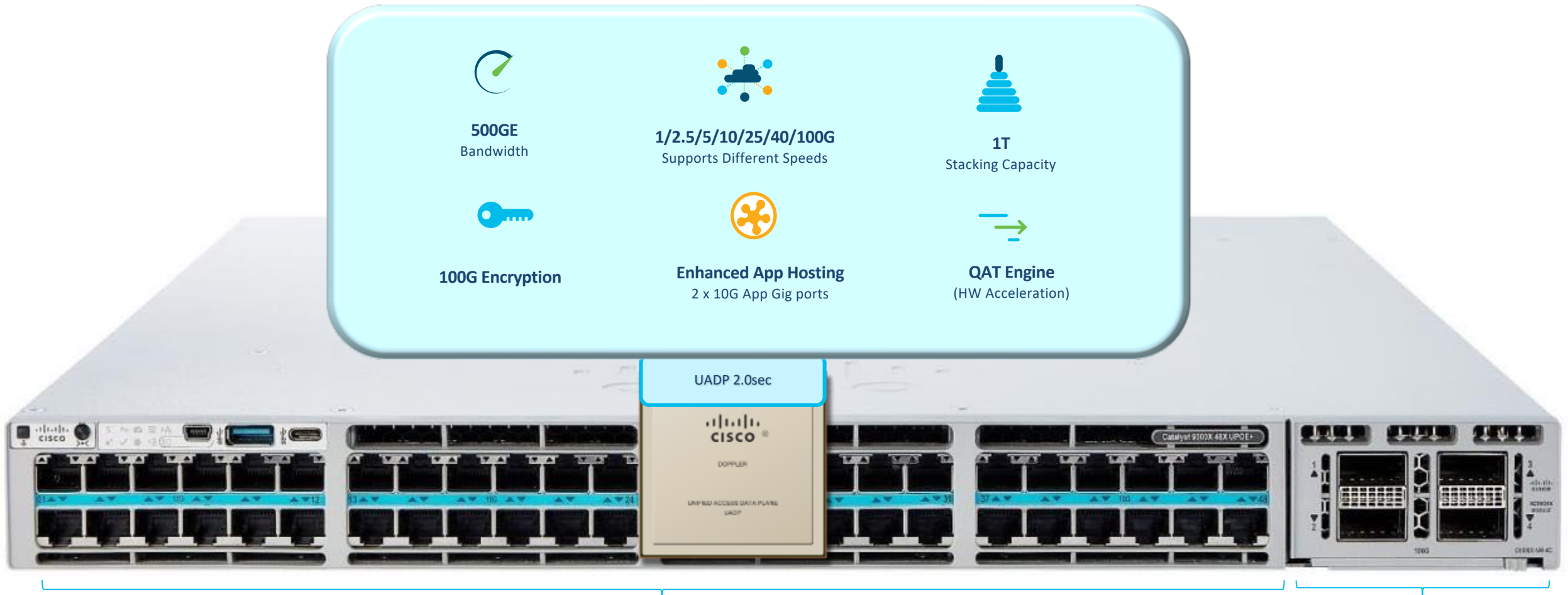


New Access requirements for Future Campus

Introducing

Catalyst 9300X

Catalyst 9300X – New High Performance Access Switch



Investment Protection with Catalyst 9300X



Common Components and Stacking Backward Compatible with Catalyst 9300

Catalyst 9300X Multigigabit Models

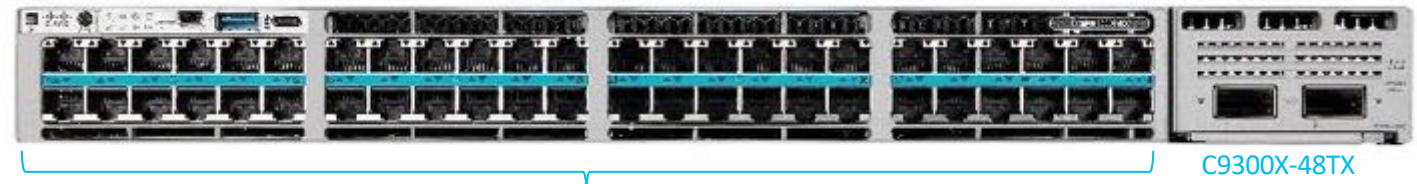
Orderable



48x 100M/1G/2.5G/5G/10G ports with **UPOE+**

C9300X-48HX

Orderable



48x 100M/1G/2.5G/5G/10G ports **Data Only**

C9300X-48TX

Roadmap
CY22

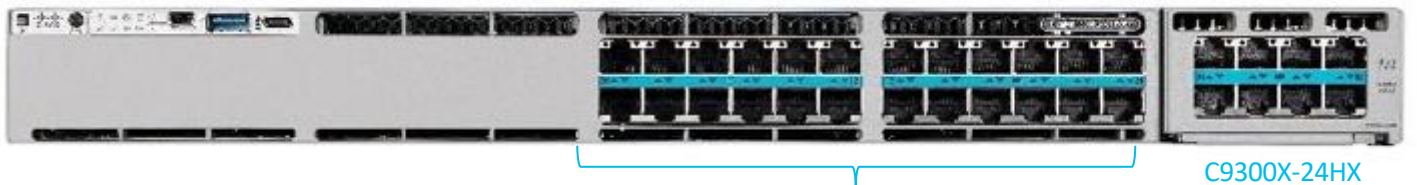


36x 100M/1G/2.5G/5G with **UPOE+**

12x 100M/1G/2.5G/5G/10G with **UPOE+**

C9300X-48HXN

Roadmap
CY22



24x 100M/1G/2.5G/5G/10G ports with **UPOE+**

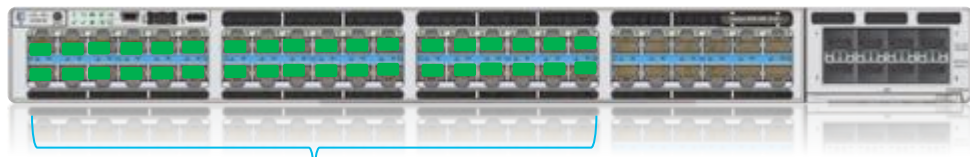
C9300X-24HX

448 mGig Ports with
8-Member Stack

Highest Multigigabit Ports in the Industry with Standalone and StackWise-1T

Highest 90W UPOE+ Density in the Industry

Standalone



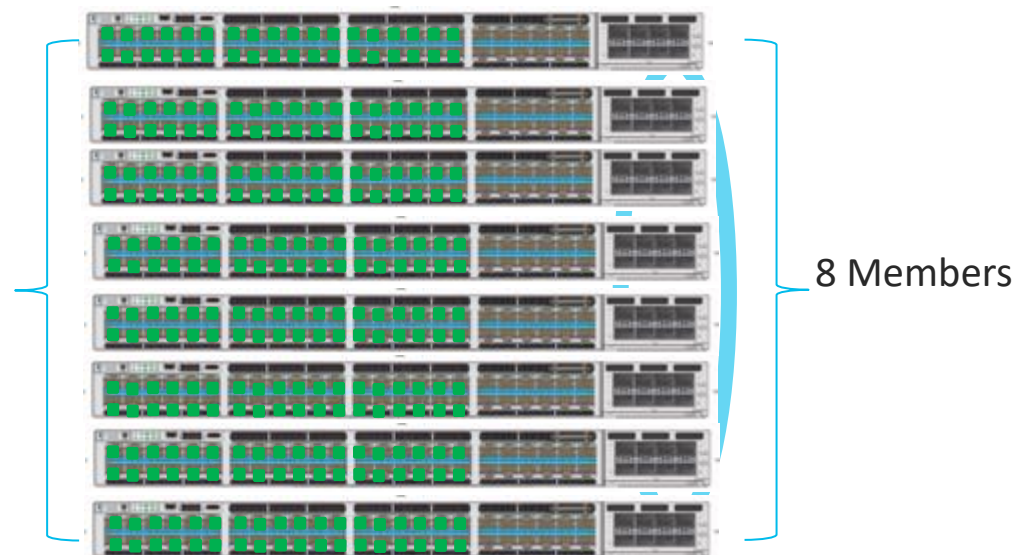
36 Ports of 90W UPOE+ or 48 Ports of 60W UPOE

36 ports of 90W or 48 ports of 60W
with 2 x 1900W AC PS/Switch

StackWise

36 Ports of 90W
UPOE+ x 8 = 288

48 Ports of 60W
UPOE+ x 8 = 384



* With Stackpower, configure 4 x 2 members for getting desired PoE Port Density

288 ports of 90W or 384 Ports of 60W
with 2 x 1900W AC PS/Switch

Highest and Flexible Speed Uplink Options in the Industry

100/40G Modular Uplinks

Roadmap
CY22

Orderable

C9300X-NM-4C

4 x 100/40G* QSFP

*Not Supported on 9300-12Y

C9300X-NM-2C

2 x 100/40G QSFP

Multigigabit Uplinks

Roadmap
CY22

C9300X-NM-8M

8 x 10G-mGig

10/25 G Modular Uplinks

Orderable

C9300X-NM-8Y

8 x 25/10/1G**

** Last 4 ports disabled on C9300X-48HXN

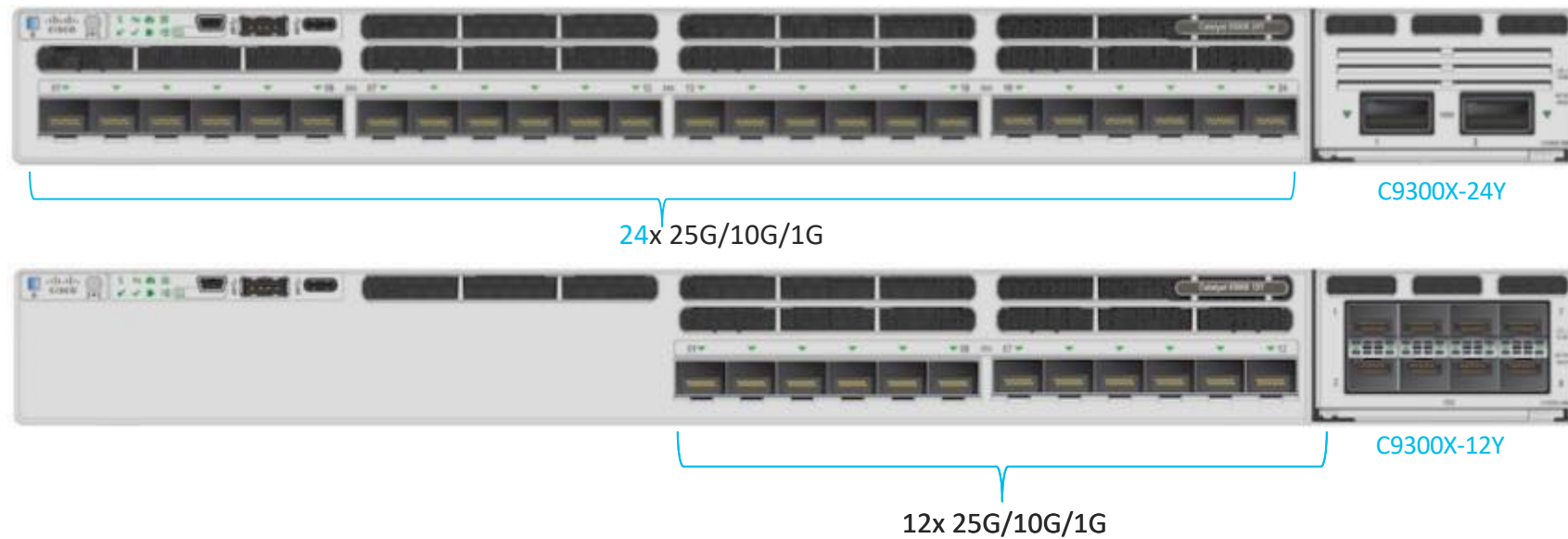
C9300X-Only Uplink modules Enabling High Speed and Port Density

Catalyst 9300X

High-Speed Fiber

Catalyst 9300X High-Speed Fiber

Shipping



Stackable with
C9300/C9300X



3850 10G Fiber
Replacement



Collapsed Access

FTTD



Servers



Bringing Stackable High-Speed fiber to the Access

Cisco Catalyst 9300 Series

Extended C9300 Family with C9300X Platform

FYI

C9300 SKUs with Modular Uplinks

1G Copper ports with PoE/UPOE/UPOE+



48/24 ports Data 1G



48/24 ports UPOE 1G



48/24 ports PoE+ 1G



48/24 ports UPOE+ 1G



48/24 ports UPOE 1G – **9300B**

2-4x
Scale/Buffer

Multigigabit Models with UPOE



48/24 ports mGig

1G Fiber Models



48/24 ports SFP 1G

C9300 Only Modular Uplinks



4x Multigigabit



4x 1G SFP



8x 1/10G SFP/SFP+



2x 1/10/25 G SFP/SFP+

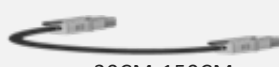


2x 40G QSFP

StackWise and StackPower Cables



50CM-1M-3M



30CM-150CM

Platinum rated power supplies



315W AC



715W AC/DC



1100W AC



1900W AC

Modular Fans



C9300X SKUs with Modular Uplinks

High Density Multigigabit Models with UPOE+



C9300X-48HX



C9300X-48TX



C9300X-48HXN



C9300X-24HX

1/10/25G Fiber Models



C9300X-24Y



C9300X-12Y

C9300X Only Modular Uplinks



4x 40/100G



2x 40/100G



8x 10/25G



8x mGig

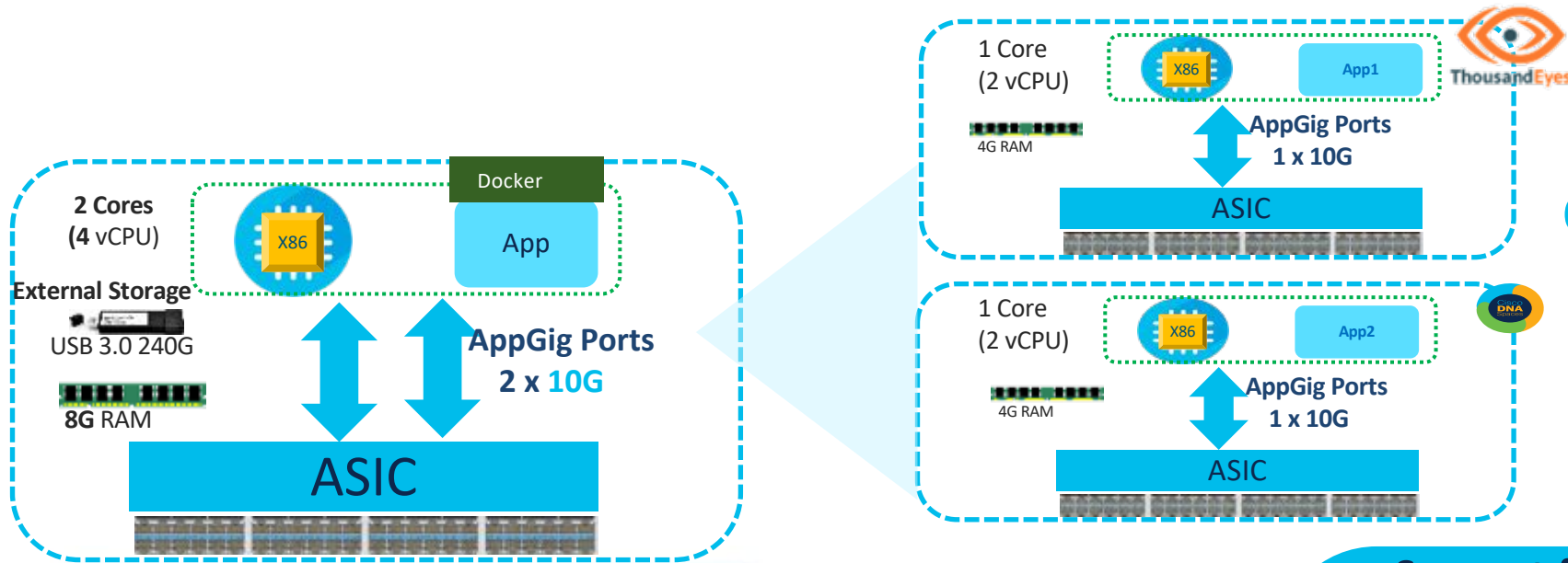
Roadmap
CY22

Orderable

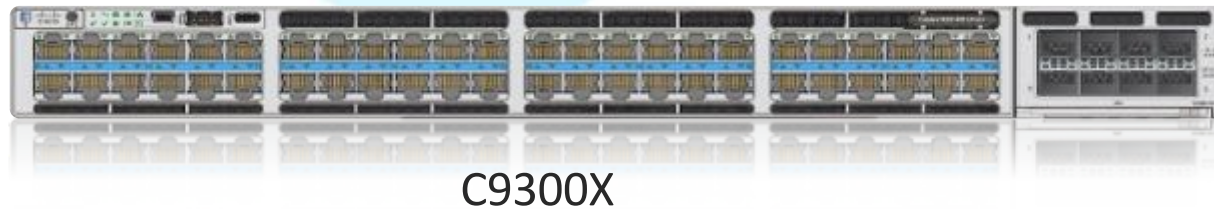
Roadmap
CY22

C9300 / C9300X App Hosting

Enhanced Application Hosting Infrastructure on C9300X



Cisco Signed Applications



Support for Multiple Docker applications

With Additional RAM Memory and 2 x AppGigabit Ports, multiple Cisco Signed performance savvy Applications can be hosted on C9300X

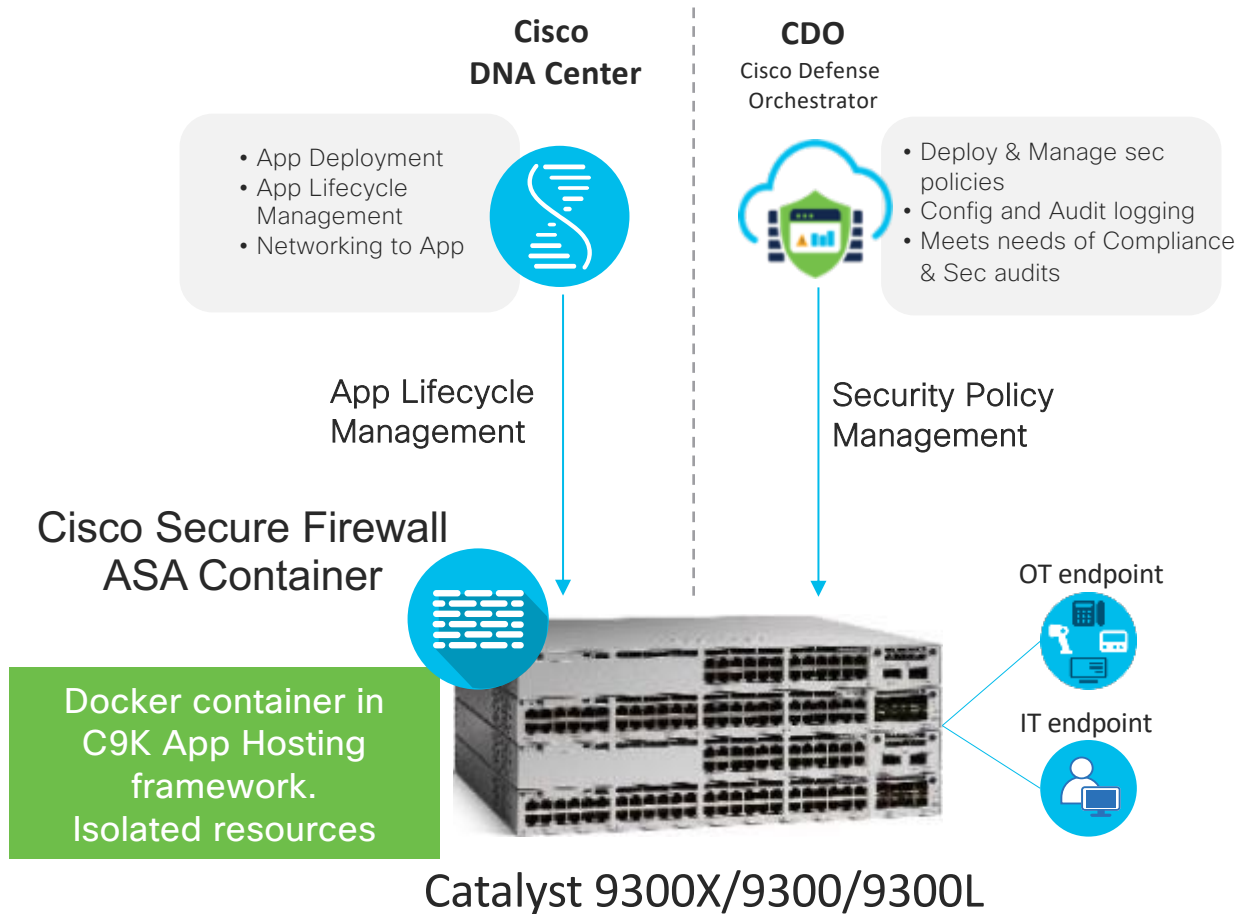
Hardware Acceleration and Security

QAT is a special engine on the x86 CPU which helps in accelerating the performance of Applications

ASAc Firewall hosted on C9K Switches

Bringing Cisco EN and Security solutions together for improved Operations

Roadmap
CY22



Use Case

- Stateful inspection of OT traffic at the Edge
 - No need of Physical Firewall
 - No need to change network architecture
 - No waste of network bandwidth
 - Automation to scale operations

- Powerful Stateful Inspection Firewall
- Separation of SecOps and NetOps
- L3 Firewall
- Support for SGT
- Expected throughput: 1 Gbps Firewall

C9300 / C9300X IPSEC

Catalyst 9300X – Purpose built for the New Edge



Cisco Catalyst 9300X

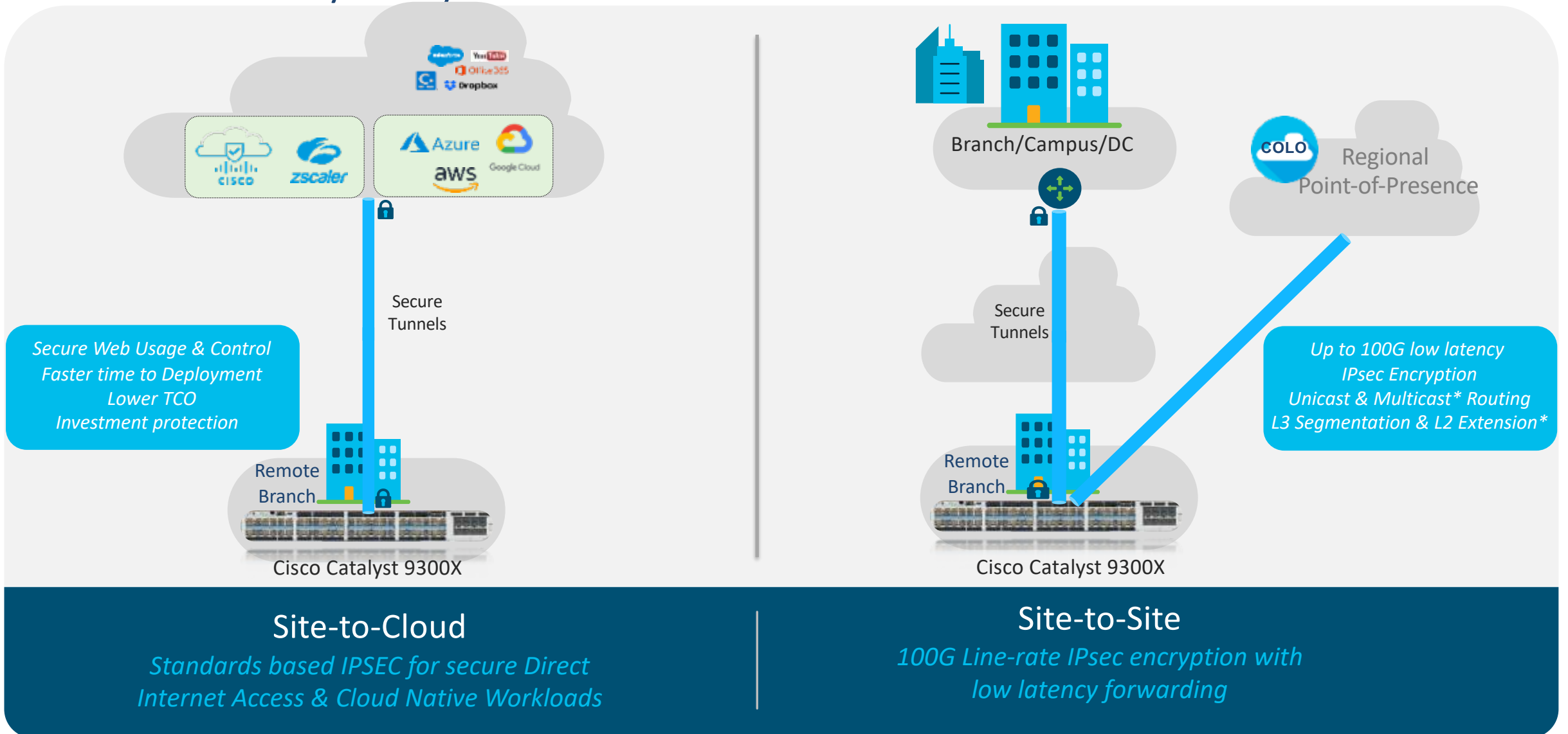
Encryption	Authentication
AES-128-CBC	HMAC/SHA1
AES-128/256-GCM	GMAC
Tunnel Mode	
Encapsulation - ESP	
IKEv2	

- | | |
|---------------------------------|-----------------------------|
| Static Virtual Tunnel Interface | NAT Traversal * |
| IPv4/IPv6 | Multicast Routing* |
| OSPF/BGP | L3 segmentation over IPSEC* |
| PBR + Set Interface * | L2 Extension over IPSEC* |

* Roadmap

Catalyst 9300X – Purpose built for the New Edge

Secure connectivity to anywhere

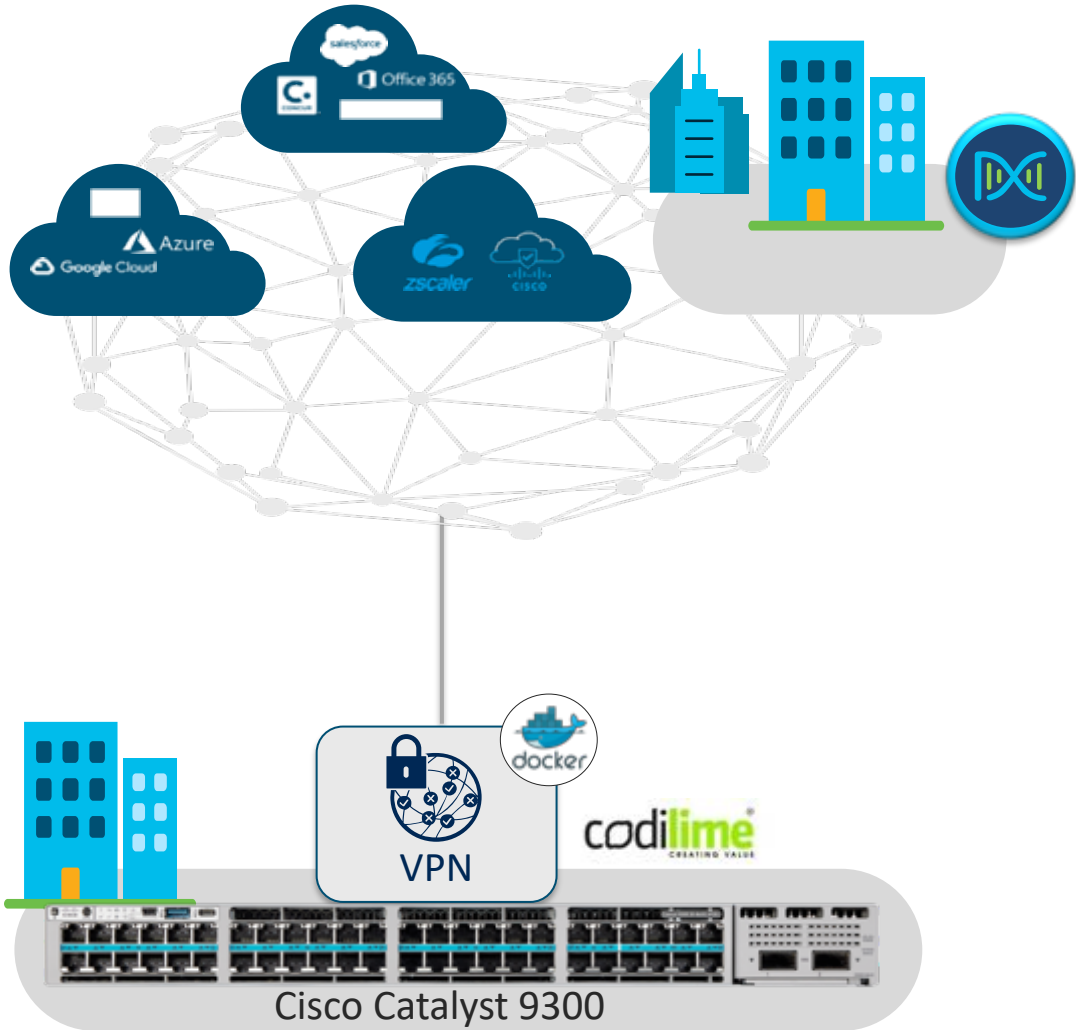


* Roadmap

New IPSEC App enabled via App-Hosting

Purpose built for IPSEC

Roadmap
CY22



- ✓ VPN Application hosted on Cat9k
- ✓ Runs in Docker container
- ✓ Web UI for IPSEC config
- ✓ Life Cycle Management via DNA Center
- ✓ HW & SW IPSEC - C9300X
- ✓ SW IPSEC - C9300/9300L
- ✓ Will be available on Devnet



- Minimal resources required
 - 1 CPU core
 - < 1 GB memory
- 200-500M throughput
- QAT for higher throughput*

IPSEC VPN
Routing



Open
Source

Expands **IPSEC** capabilities to all **9300 models** at lower throughput

* On 9300X Models





Introducing

Catalyst 9300LM


Cisco Catalyst 9300LM Series

Fixed uplink replacement for Catalyst 3650-mini




 <p>8 mGig Ports, 4x25G Uplink</p> <p>48 Port mGig UPOE</p>	 <p>4x25G Uplink</p> <p>48 Port 1G UPOE</p>
 <p>4x25G Uplink</p> <p>48 Port 1G Data</p>	 <p>4x25G Uplink</p> <p>24 Port 1G UPOE</p>


Cisco Catalyst 9000 leadership
Same UADP performance as C9300L
Cisco IOS® XE Software
SD-Access
x86 CPU and containers
Encrypted Traffic Analytics (ETA)
AES-256/MACsec-256
Trustworthy systems
Cisco StackWise-720*/320
IEEE1588 and AVB
NBAR2
Perpetual/Fast PoE
Model-driven programmability
Patching/GIR
Streaming telemetry
NEBS L3 Certified




UADP 2.0




Multicore X86 CPU




Open IOS XE




USB type-A Front Panel SSD*




Stackable with C9300L



mGig



802.3bt Type-3



25G Ready

Modular fans*

Modular Stacking

Higher-efficiency AC and DC power supplies



600W AC 715W DC 1000W AC



Platform Depth <14 inches		
	AC PSU	DC PSU
UPOE	13.2 in	12.8 in
Data	12.4 in	12.0 in

Note: *Data SKU utilize fixed fans

Introducing

Catalyst 9400X

Cisco Catalyst 9400X

New Supervisor 2/2XL powered by Cisco UADP 3.0sec ASIC

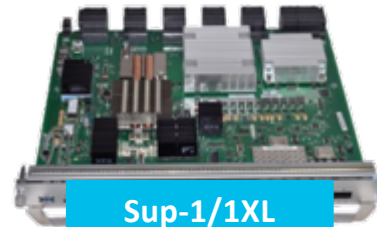
Sup1-XL Feature Parity at FCS

Exceptions
(Roadmapped)

- StackWise Virtual
- Perpetual and Fast PoE
- MACsec HA on LC
- MACsec XPN Support on SUP
- Auto Neg on Passive cable

UADP 3.0sec

UADP 2.0XL



Sup-1/1XL



Sup-2/2XL

480Gbps/Slot with Sup-2XL
240Gbps/Slot with Sup-2



Up to 240G
bandwidth

1/2.5/5/10/25/40G
Supports Different Speeds

Forwarding + ACL Scale
Up to 96K MACs
Up to 64K Routes

Up to 32 MB
(2 x 16MB) packet
buffer

240/120/80Gbps/Slot with Sup-1XL (4/7/10 Slot
Chassis)
80Gbps/Slot with Sup-1 (All Chassis)

Up to 1.6T
Bandwidth

1/2.5/5/10/25/40/100G
Supports Different Speeds

**Increased
Forwarding + ACL Scale**
Up to **128K MACs***
Up to **256K Routes***

Up to 36 MB
Unified packet
buffer

Up to 100G
Encryption
IPSec*, WAN-MACsec*

Customizable
Templates for
higher Scale*

* Hardware Capable, Software Support not committed

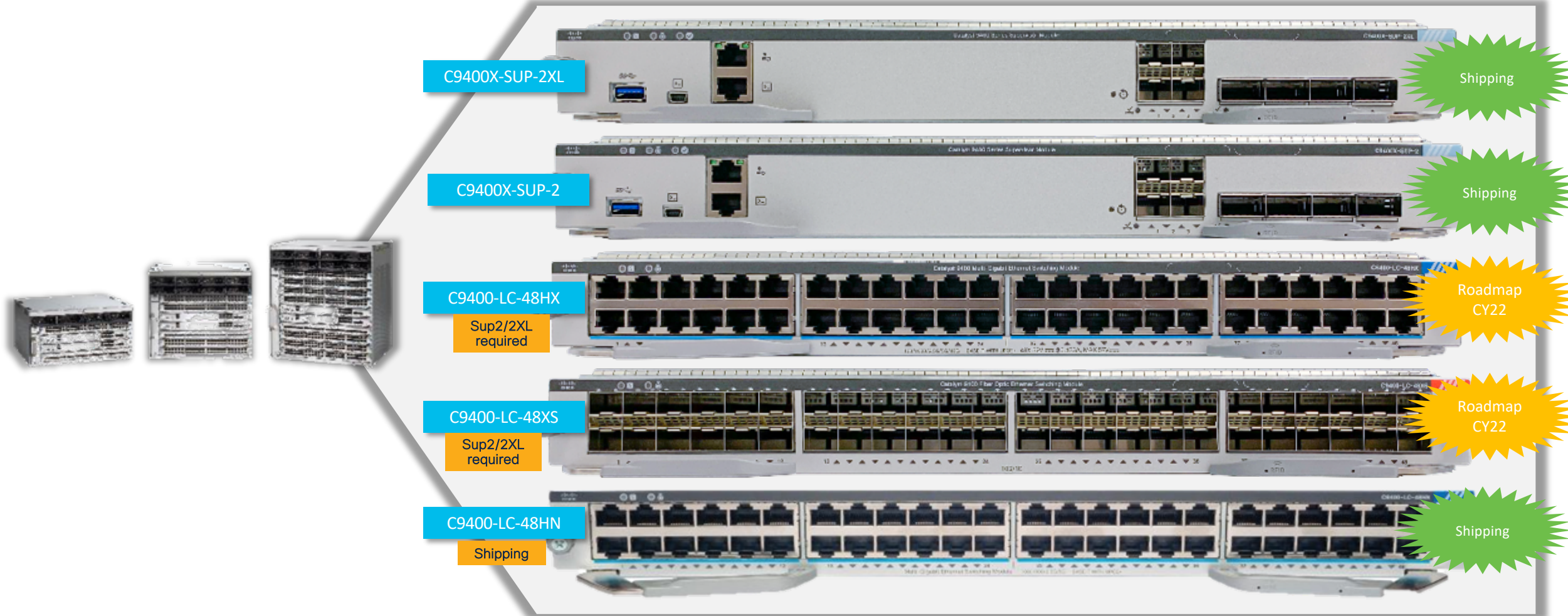
Unmatched Flexibility

Maximum Investment Protection

100G Leadership in Access

Same Series, Chassis options – New SUPs and Line cards

Same Chassis with New Supervisors and Line cards



Bandwidth Boost with Gen2 Supervisors



Cisco C9400 SUP 1/1XL

Cisco C9400X SUP2

Cisco C9400X SUP2XL

	Type	C9404R	C9407R	C9410R	C9404R/C9407R/C9410R	C9404R/C9407R/C9410R
New C9400-LC-48HX	UPOE+	-	-	-	240	480
New C9400-LC-48XS	Fiber	-	-	-	240	480
C9400-LC-48UX	UPOE	80 / 240	80 / 120	80	240	240
C9400-LC-24XS	Fiber	80 / 240	80 / 120	80	240	240
C9400-LC-48HN	UPOE+	80 / 120	80 / 120	80	240	240

Bandwidth in Gbps

Bold indicates Line Rate

3x Bandwidth Uplift for Gen1 LCs (**80G -> 240G**) on **10 Slot Chassis w/ SUP2XL**

2x Bandwidth Uplift for Gen1 LCs (**120G -> 240G**) on **7 Slot Chassis w/ SUP2XL**

Concurrent 60W/90W POE Port Density with C9400-LC-48HX

With **3200W** Power Supply in Combined Mode(Fully loaded PSUs):

C9410



C9407



C9404



	C9404	C9407	C9410
Total Ports	96 ports	240 ports	384 ports
UPOE + 90W	96 ports (Fully loaded chassis)	226 ports (Up to 4 fully loaded LCs + 34 Ports)	224 ports (Up to 4 fully loaded LCs + 32 Ports)
UPOE 60W	96 ports (Fully loaded chassis)	240 ports (Fully loaded chassis)	336 ports (Up to 7 fully loaded LCs)

Distribution / Core



Addressing the Campus Core + Edge Market

More than just “Speeds & Feeds”



System Capacity

- **Higher Port Speeds**
enabling newer Ethernet speeds and types, such as 50G SFP and 400G QSFP
- **More Access Bandwidth**
higher density of 802.11ac moving to 11ax, HD Video (1080p) moving to UHD (4K)
- **Non-Blocking**
Core needs non-blocking (1:1) performance



System Scale

- **High-Scale Routing**
support for full IPv4 and IPv6 Internet + LAN + VRF routing
- **Flexible Transport Options**
support for MPLS-VPN, SD-Access and BGP-EVPN with 4K VRFs
- **Centralized Wireless**
support for high MAC and ARP/NDP scale



Port Density

- **More Uplinks**
support for multiple QSFP uplinks, with LR/ZR optics for redundant edge connections
- **More Downlinks**
support for hundreds of SFP ports/breakouts
- **Port Options**
mix of SFP & QSFP ports, at various interface speeds



QoS & Buffers

- **Low-Latency Buffers**
support for local optimized low-latency shared memory
- **High-Bandwidth Memory**
support large buffers for micro-burst & congestion
- **Virtual Output Queuing**
eliminate head-of-line blocking, with dedicated output queues for every egress port



Flexibility

- **Programmable ASIC**
Enable new features and encapsulations
- **Model-driven Microcode**
hardware functions use model-driven APIs
- **App Hosting Infra**
support Docker applications
- **System-level HA**
L2/L3 redundancy with Stackwise Virtual and GIR



Core + Edge



Core + Distro



Extending Cisco Catalyst 9500 & 9600 Series

Powered by Cisco Silicon One™ Q200 ASIC



C9500 & C9600-SUP1 (w/ UADP 3.0)

Optimized for Features

- ✓ **Speed**
 - 1/10 & 25G SFP
 - 40 & 100G QSFP
- ✓ **Scale**
 - Upto 128K MACs
 - Upto 256K Routes
 - 108MB Buffers (3x 36MB)
- ✓ **Services**
 - L2/L3 Routing, MPLS
 - LAN MACsec, Netflow, NAT
 - Custom ASIC Templates
 - Campus Fabric (SDA & EVPN)

Double Existing
Throughput



WAN MACsec,
1588v2 PTP



C9600X-SUP-2
C9600-LC-40YL4CD



10^x

Routing &
MPLS Scale



C9500X-28C8D



80MB Low-Latency +
8GB High-BW Buffers



50GE, 400GE,
Coherent DWDM



C9500X & C9600X-SUP2 (w/ S1 Q200)

Optimized for Scale

- ✓ **Speed**
 - 10/25G & **50G**** SFP
 - 40/100G & **200**/400G** QSFP
- ✓ **Scale**
 - Upto **256K** MACs
 - Upto **2M** Routes
 - **80MB + 8GB** Buffers
- ✓ **Services**
 - L2/L3 Routing, MPLS/TE
 - LAN & **WAN-MACSec***, Netflow, NAT**
 - Custom ASIC Templates
 - Campus Fabric (SDA & EVPN**)

Maximum Investment Protection

400G Leadership in Campus

Unmatched Flexibility

Catalyst 9000 Series – Common Building Blocks



Programmable x86
Multi-Core CPU

Application Hosting
Secure Containers



Open IOS XE[®]
Polaris

Model-Driven APIs
Modular Patching



Cisco Silicon One[™]
Q200 ASIC

Programmable Pipeline
Flexible Tables

Same IOSXE image for both UADP* and Silicon One C9K platforms

Introducing

Catalyst 9500X

Catalyst 9500 Series

Extending High-Performance Fixed Core with a Performance-Optimized Edge Switch

Non-XL Scale

Catalyst 9500H
(UADP 3.0)



C9500-32C / C9500-32QC



C9500-48Y4C / C9500-24Y4C

Total Capacity

3.2 Tbps

32 x 100G or
48 x 25G + 4 x 100G



Core, Edge, DCI, Colo



XL Scale

Catalyst 9500X
(S1 Q200)



C9500X-28C8D

Total Capacity

6.0 Tbps

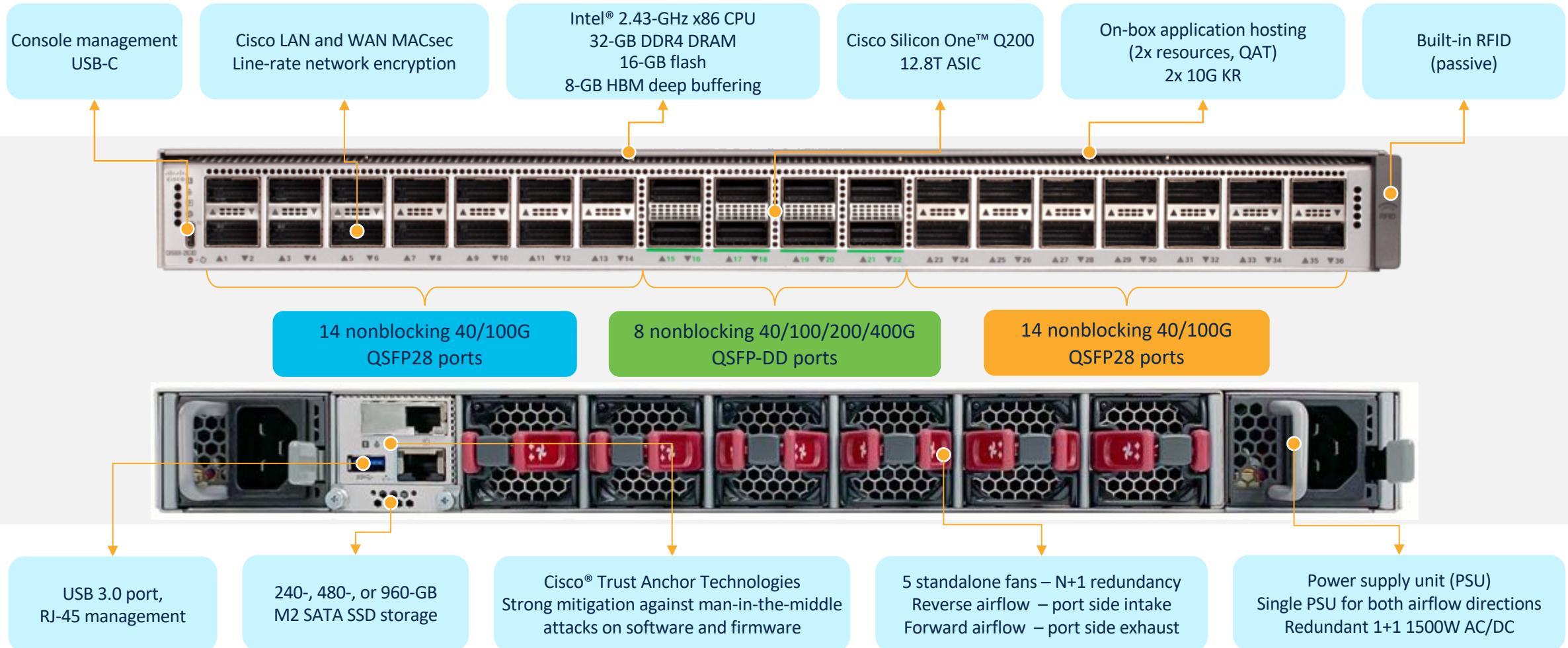
36 x 100G or
28 x 100G + 8 x 400G

2x

Cisco Catalyst C9500X-28C8D

High-level overview

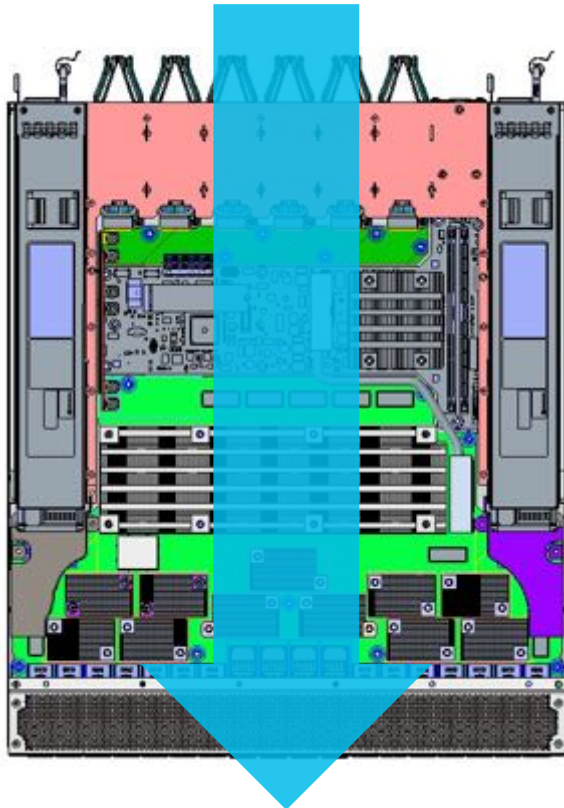
Available since Feb 2022



C9500X – Reversible Airflow



Back to Front
Port-side Exhaust

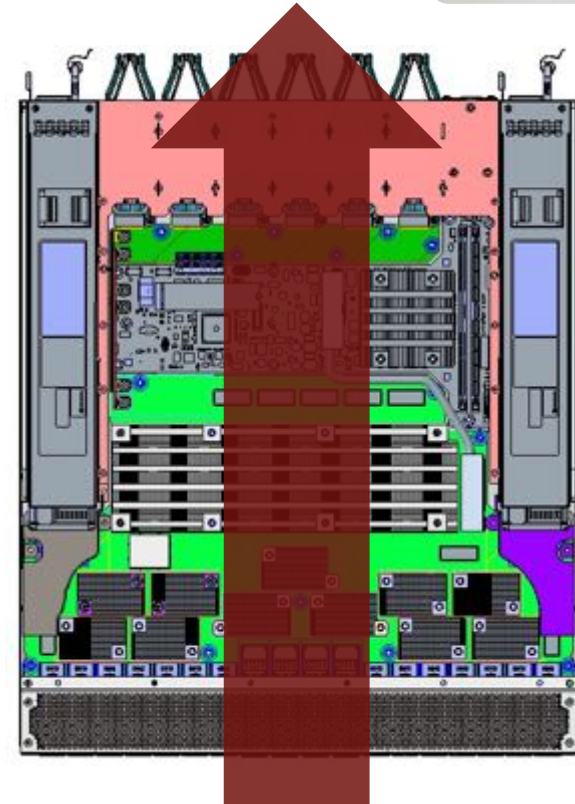


- Color of Fan Unit handle/latch represents direction of airflow
- Different Fan PIDs for different airflow directions
 - **Royal Blue** – Back to Front
 - **Burgundy** – Front to Back
- All Fans must be the same color (direction) to work correctly



Single 1500W AC/DC PSU
with Cisco Grey latch
for both airflow directions

Front to Back
Port-side Intake



Introducing

Catalyst 9600X

Catalyst 9600 Series

Extending Modular Core with a Performance-Optimized Supervisor & Cards

UADP 3.0



Supervisor 1

Total Capacity

4.8 Tbps

Slot B/W

1.2 Tbps



SSD

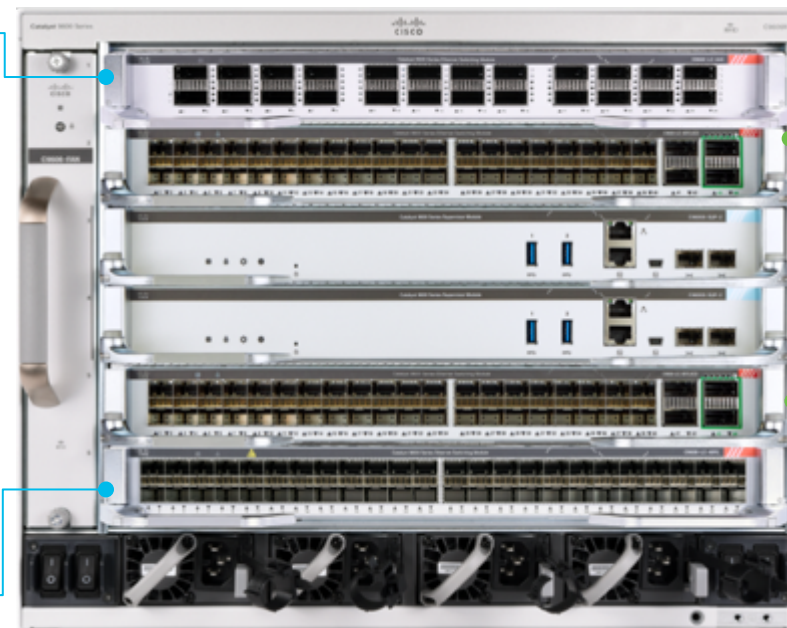


Fan-Tray



PSU

Gen1
1.2T /slot



Gen1
1.2T /slot

Gen2
3.2T /slot

Gen2
3.2T /slot

400G

40x 1/10/25/50G + 2x 200G + 2x 400G

NEW



SiliconOne
Q200

NEW

Supervisor 2

Total Capacity

12.8 Tbps

Slot B/W

3.2 Tbps

3x

Catalyst 9600X: Introducing the first 400G line card in campus

Shipping

Catalyst® 9606R



C9600-LC-24C



C9600-LC-48YL



C9600-LC-48S



C9600-LC-48TX
(Multigigabit)

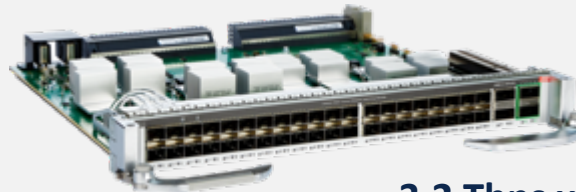


Combo line card

NEW

C9600-LC-40YL4CD

40x SFP56 +
2x QSFP56 + 2x QSFP-DD



3.2 Tbps with SUP-2
1.2 Tbps with SUP-1

Provides for **uplink requirement**
without using additional slot



Dual-personality
line card



Flexible speed
support



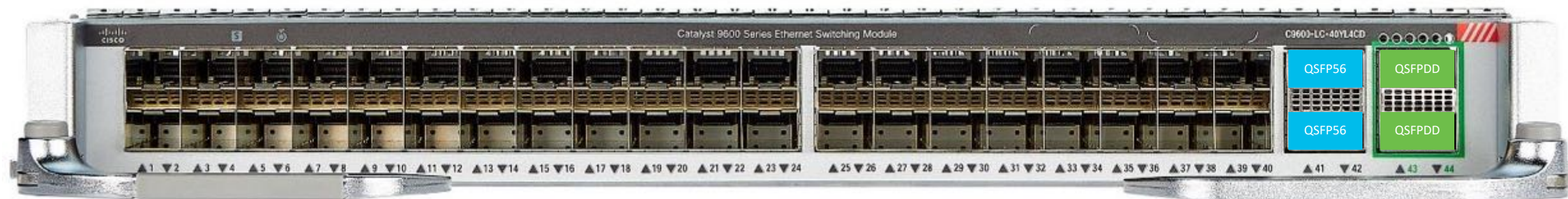
Lower total BoM
cost, save on
additional line cards

C9600-LC-40YL4CD Ports and Speeds Support

with Sup2: 3.2Tbps

40x 10/25/50*GE + 2x 40/100/200*GE + 2x 40/100/200*/400GE

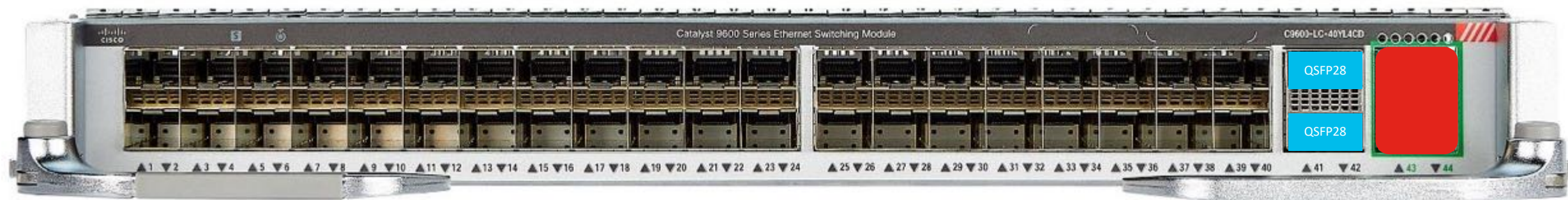
IOS-XE 17.7.1



with Sup1: 1.2Tbps

40x 1/10/25GE + 2x 40/100GE

IOS-XE 17.8.1



* Roadmap (not committed).

Catalyst 9600 line card and supervisor support matrix

	SUP-1	SUP-2
C9600-LC-24C	✓ 24x 40G or 12x 100G	✓ 24x 40G and 100G (No MACsec)
C9600-LC-48YL	✓ 48x 1/10G and 25G	✓ 48x 10/25G and 50G* (No MACsec, no 1G)
C9600-LC-48TX	✓ 48x 1/2.5/5G and 10G (Multigigabit)	✓ 48x 10G (No MACsec, no 1/2.5/5G)
C9600-LC-48S	✓ 48x 1G SFP	✗
C9600-LC-40YL4CD	✓ 40x 1/10G and 25G + 2x 40G and 100G	✓ 40x 10/25G and 50G* + 2x 40/100G and 200G* + 2x 40/100/ 200G* and 400G MACsec and WAN MACsec (no 1G)



SUP-2 does not support speeds of 1G or below

If 1G downlinks are required, position SUP-1

Introducing

Cisco Silicon One™

Cisco Silicon One™



Switching Silicon

- **High Throughput**
extremely fast hardware-based L2-L4 forwarding and services (measured in Terabits per second)
- **Optimized Scale**
optimized for Campus LAN environments with moderate IP & MAC scale (10s-100s of thousands)
- **Low Latency**
extremely low hardware-based system latency (measured in Nanoseconds & Microseconds)
- **Streamlined Buffering**
shallow buffering systems to reduce latency, with very high throughput



Routing Silicon

- **Flexible Features**
complex, stateful L3-L7 forwarding and services (measured in Gigabits per second)
- **Massive Scale**
optimized for WAN/SP environments with very high IP scale (100s of thousands - millions)
- **Mixed Interfaces**
support for Ethernet, Serial, Cellular and other types and speeds in a single system
- **Deeper Buffering**
deep buffers to accommodate different speeds, bursts and different flow patterns

Cisco Silicon One Bringing Switching and Routing convergence

Cisco Silicon One™ Q200

Industry leading Switching and Routing Silicon



12.8T BW



8.1 Bpps



8G HBM for
deep buffers



10M IPv4
or 5M IPv6
route scale



Fully P4
Programmable
Pipeline



50G PAM4
Serdes

Cisco Silicon ONE Q200

Industry Leading 12.8T System on Chip



First 7nm ASIC providing lowest
watts/GE power consumption



Fully P4 programmable enabling
feature velocity

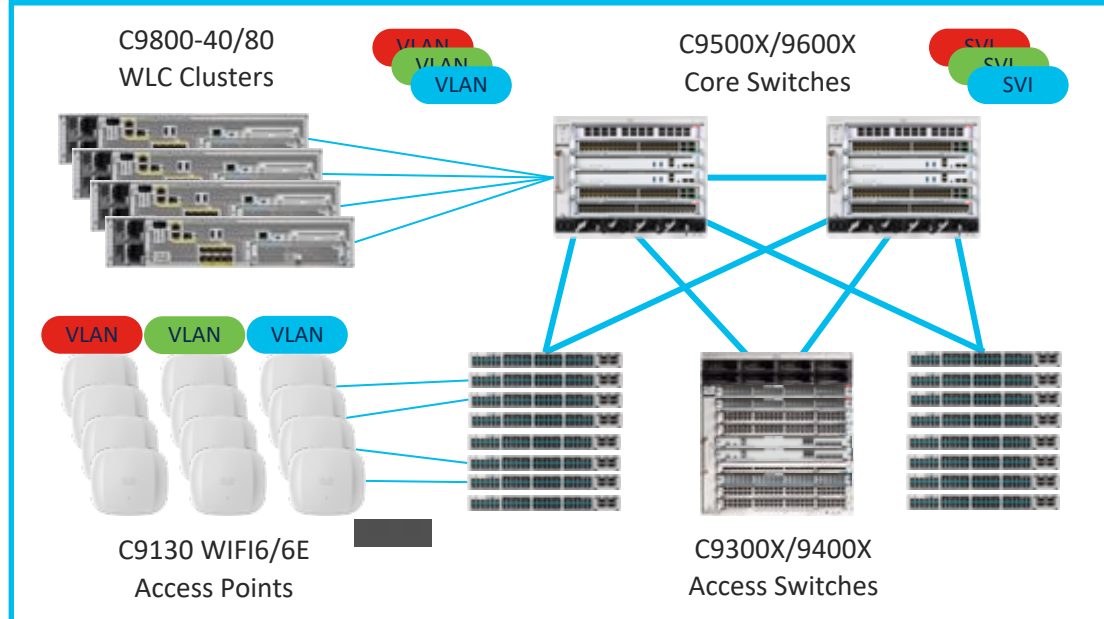


Multi slice architecture for
flexibility and scale

Routing Capabilities with Switching Power and Performance

Why bigger L2 & L3 in Campus Core?

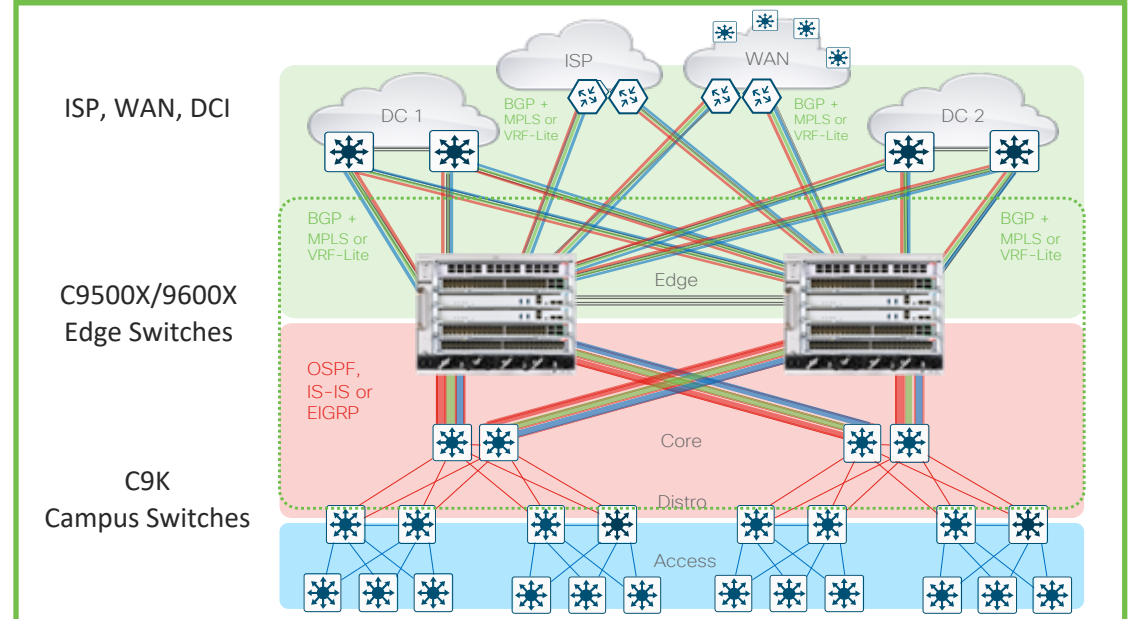
Central Wireless



WLCs (Clusters) connected centrally to Core

- 32K Clients = 32K IPv4 + 96K IPv6 = ~128K
- 802.1Q trunks from WLC to Core
- Wireless LANs (VLANs) carried over trunk
- SVIs reside on Core (1st Hop L3 Gateway)
- Core must resolve all MAC & ARP/NDP

Internet & Edge Routing



Core connected to Internet Service Provider

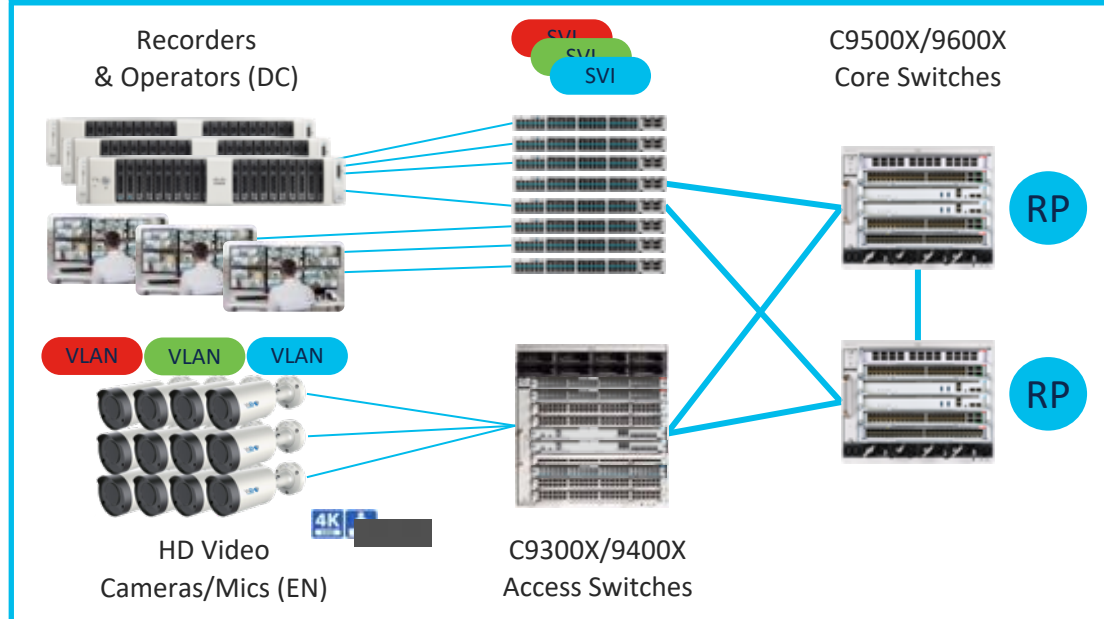
- Current Internet Tables: ~850K IPv4, ~50K IPv6
- 2x Neighbors, MP-BGP peering, BFD, NSF, GIR

Core connected to Enterprise MAN / WAN

- 1000 per VRF x ~1000 VRF = ~1M routes
- 8x Neighbors, IGP, BGP, MPLS, SDA/EVPN, QinQ

Why flexible Multicast in Campus Core?

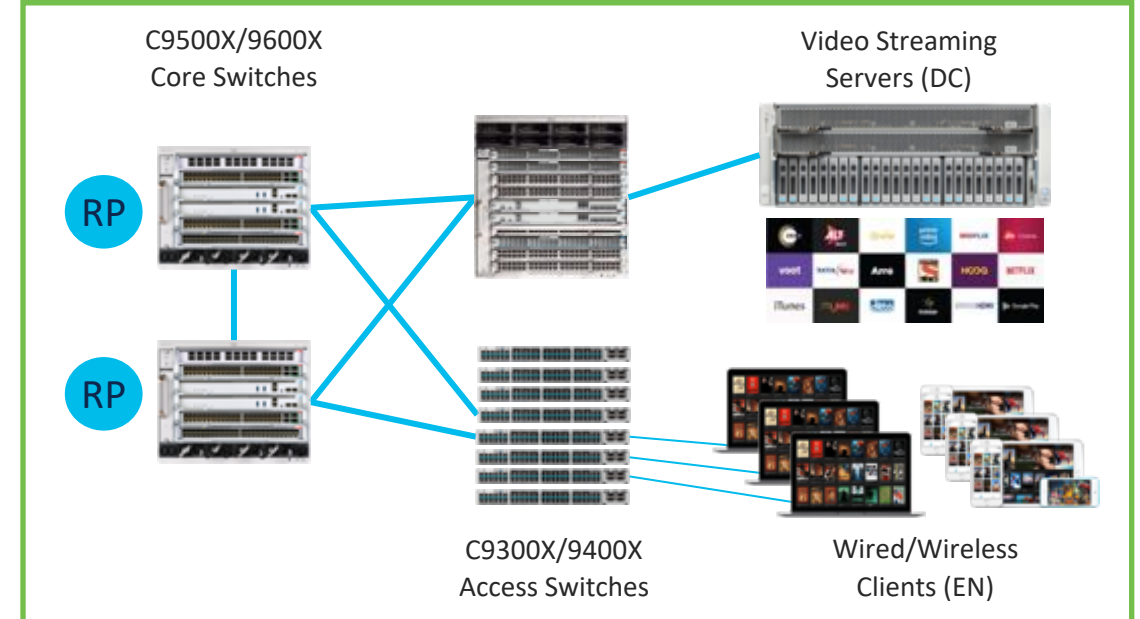
Voice & Video Surveillance



Geo-separated distribution of real-time Audio/Video

- 10,000's of HD Cameras / Microphones
- 100-1000's of Receivers (Recorders & Operators)
- Different locations of Recorders & Operators
- IPv4 & IPv6 PIM-SM and Bidir PIM
- Multicast VPN (Rosen, mLDP) for Security

Streaming & On-Demand

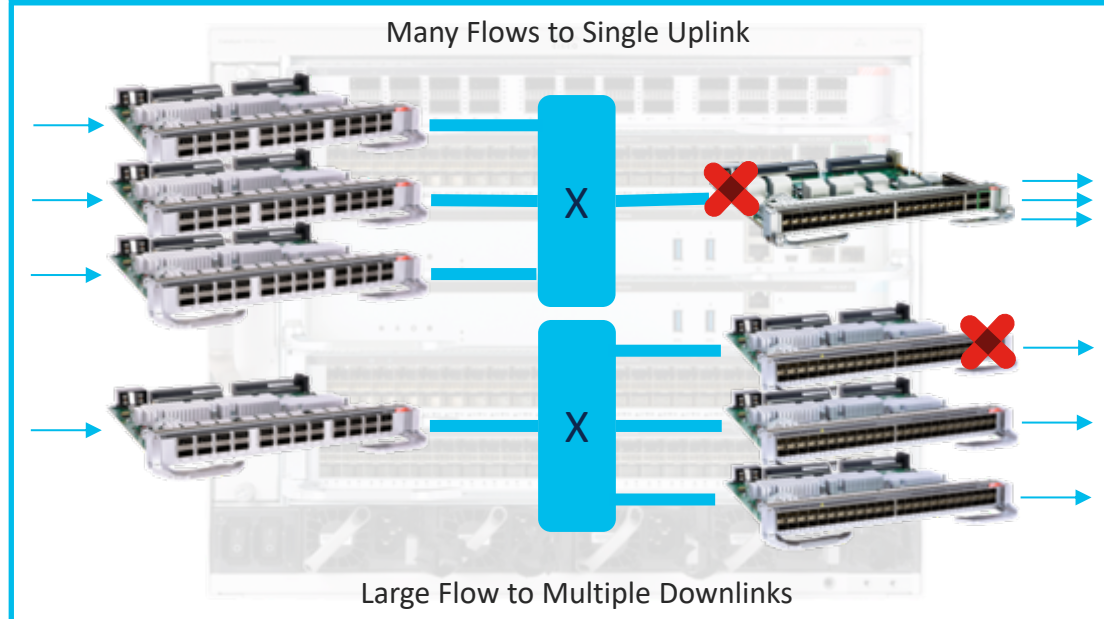


Massive scale & performance for VOD Streaming

- 10,000's of Receivers (wired & wireless)
- 100-1000's of On-demand Videos
- Special QoS queueing & buffering for A/V data
- IPv4 & IPv6 PIM-SM and PIM-SSM
- IGMPv3 & MLDv2 and explicit host-tracking

Why VoQ QoS in Campus Core?

No Head-of-Line Blocking



Many Flows to a Single Uplink

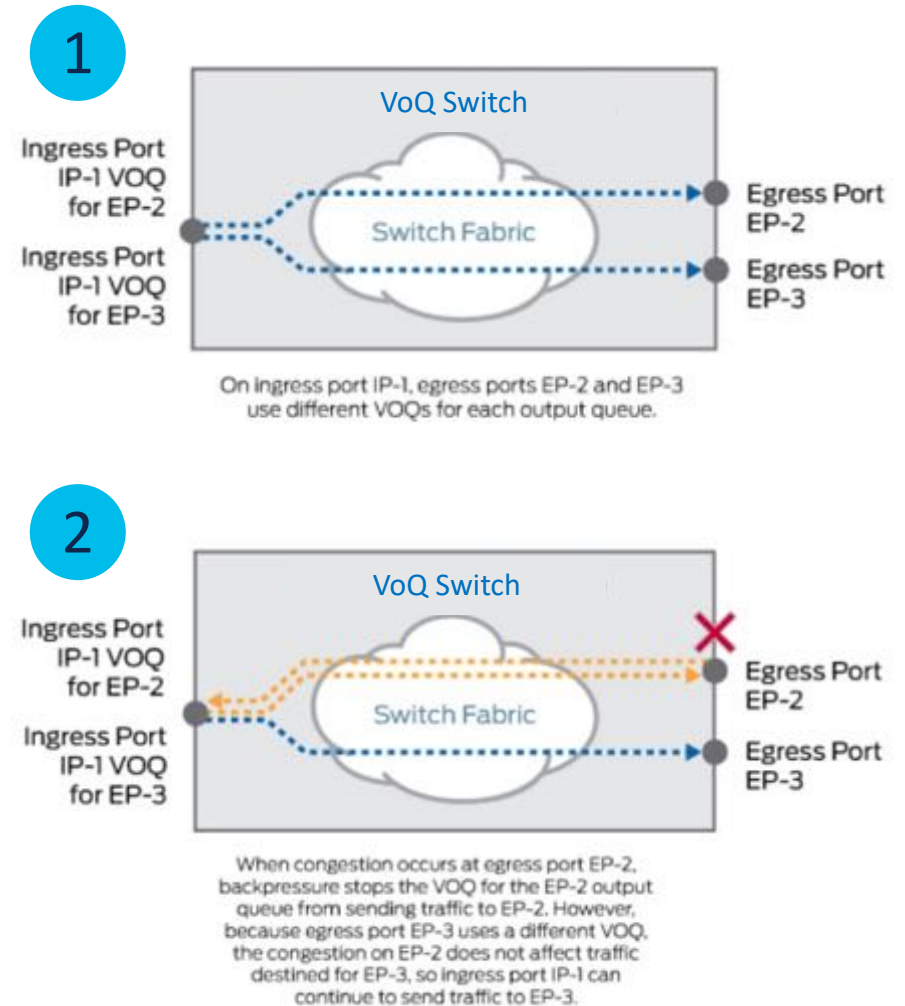
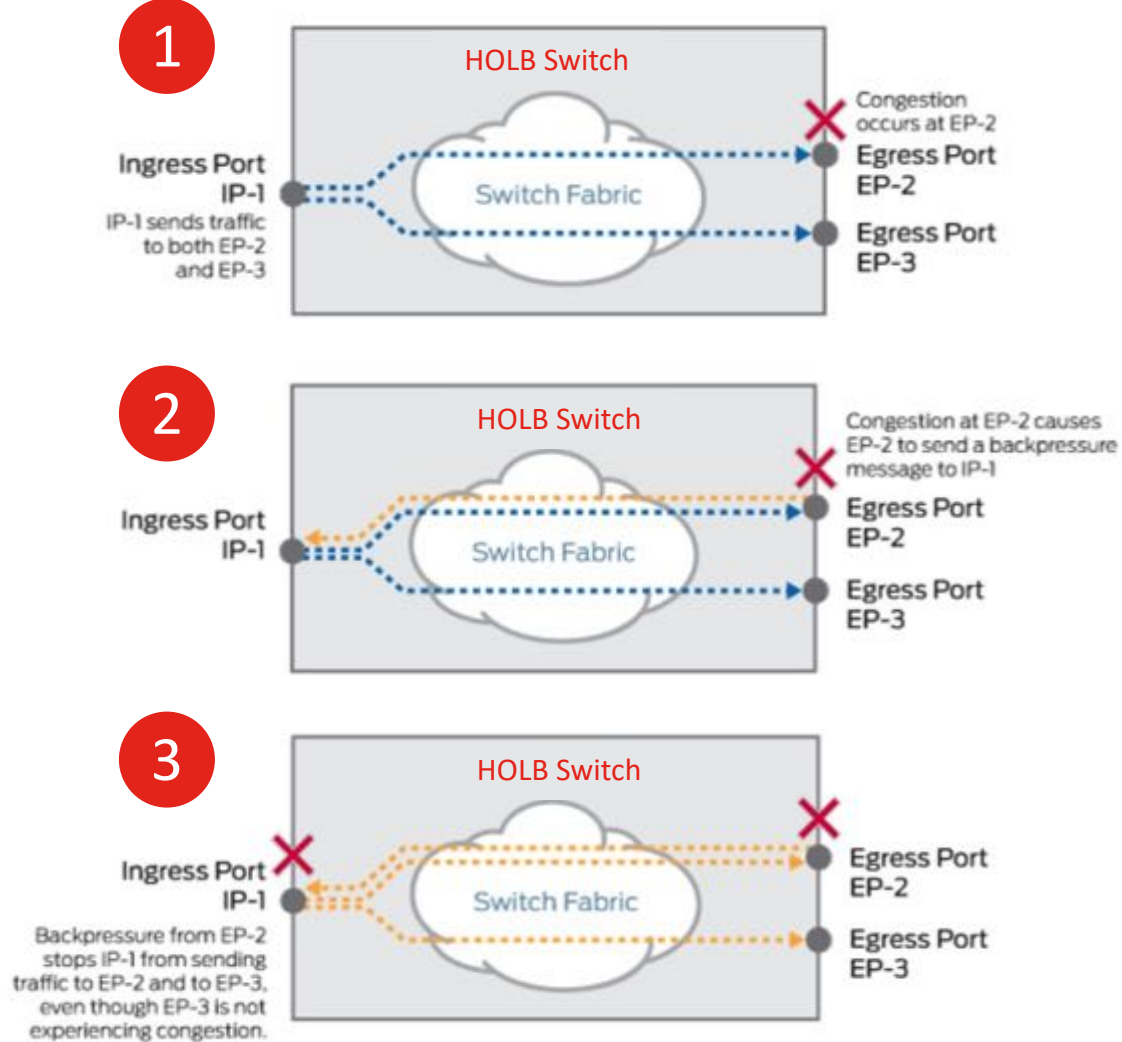
- Common on (expensive) WAN/Edge uplinks
- Even if bandwidth available, buffers can fill up

Large Flow to Multiple Downlinks

- Common for Multicast & Broadcast traffic
- One slow receiver can penalize other ports

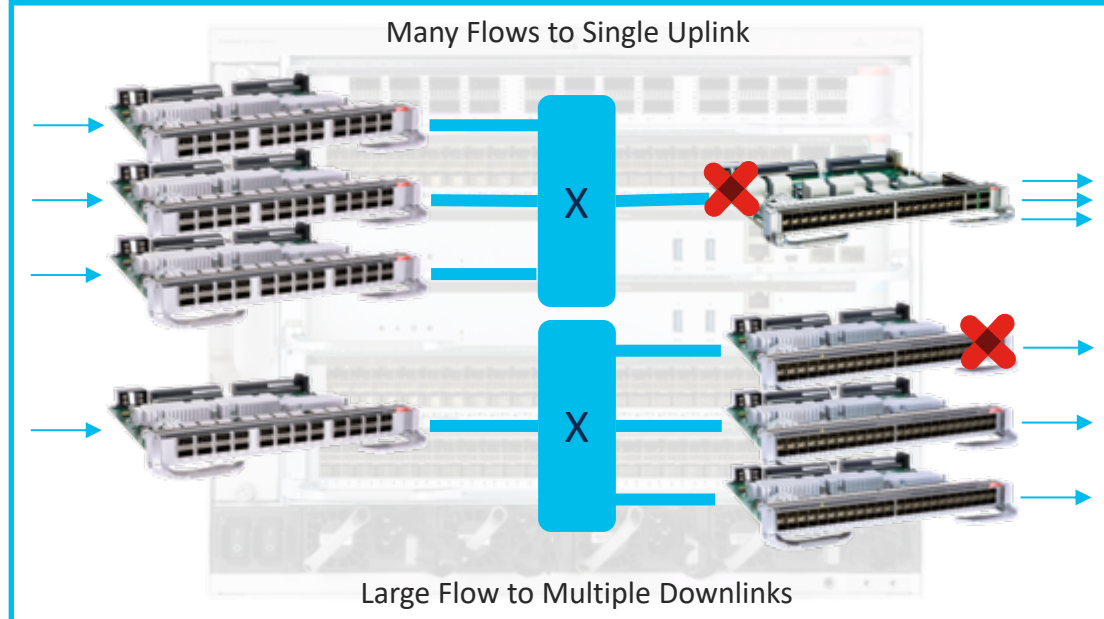
Why VoQ Architecture?

Virtual Output Queueing – Egress Optimized



Why VoQ QoS in Campus Core?

No Head-of-Line Blocking



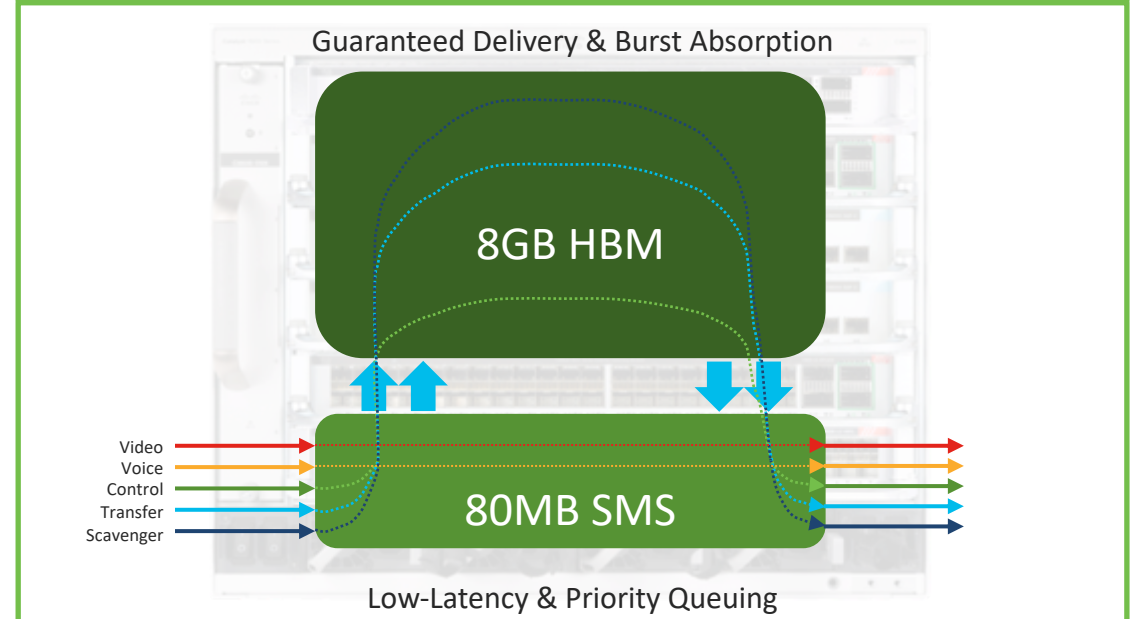
Many Flows to a Single Uplink

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Large Flow to Multiple Downlinks

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Local vs. HBM Buffers



Low-Latency Local Shared Memory Buffers

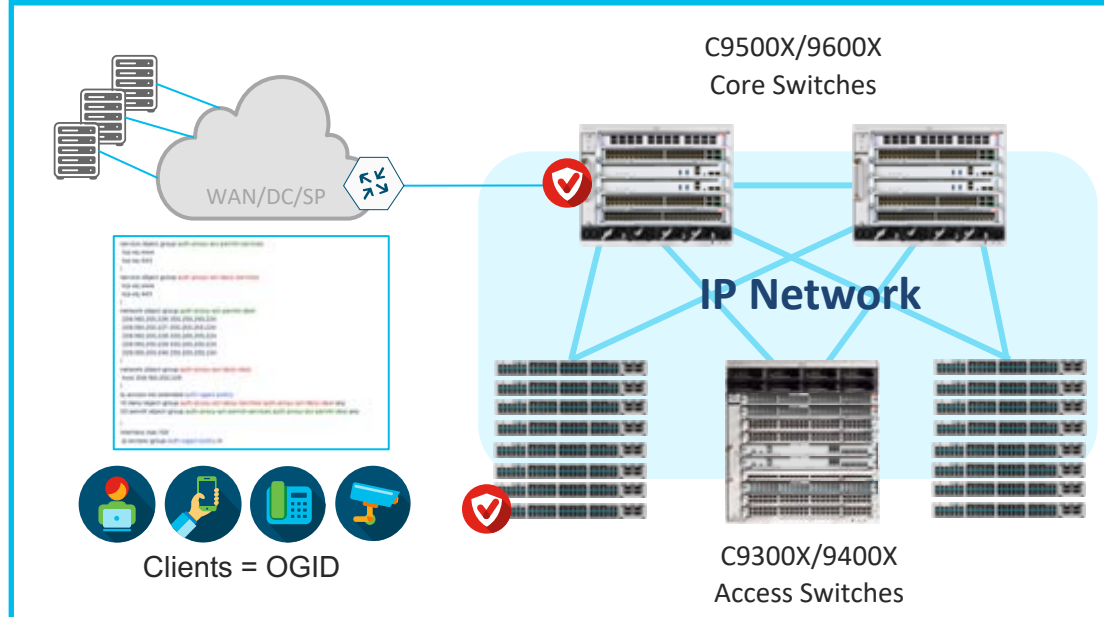
- Voice & Video are very latency-sensitive
- Multiple levels of Strict Priority Queuing

Deep High-Bandwidth Memory Buffers

- Guarantee delivery of session-oriented flows
- Reserve buffers to absorb occasional bursts

Why OGACL/SGACL in Campus Core?

Object-Group ACLs for IP



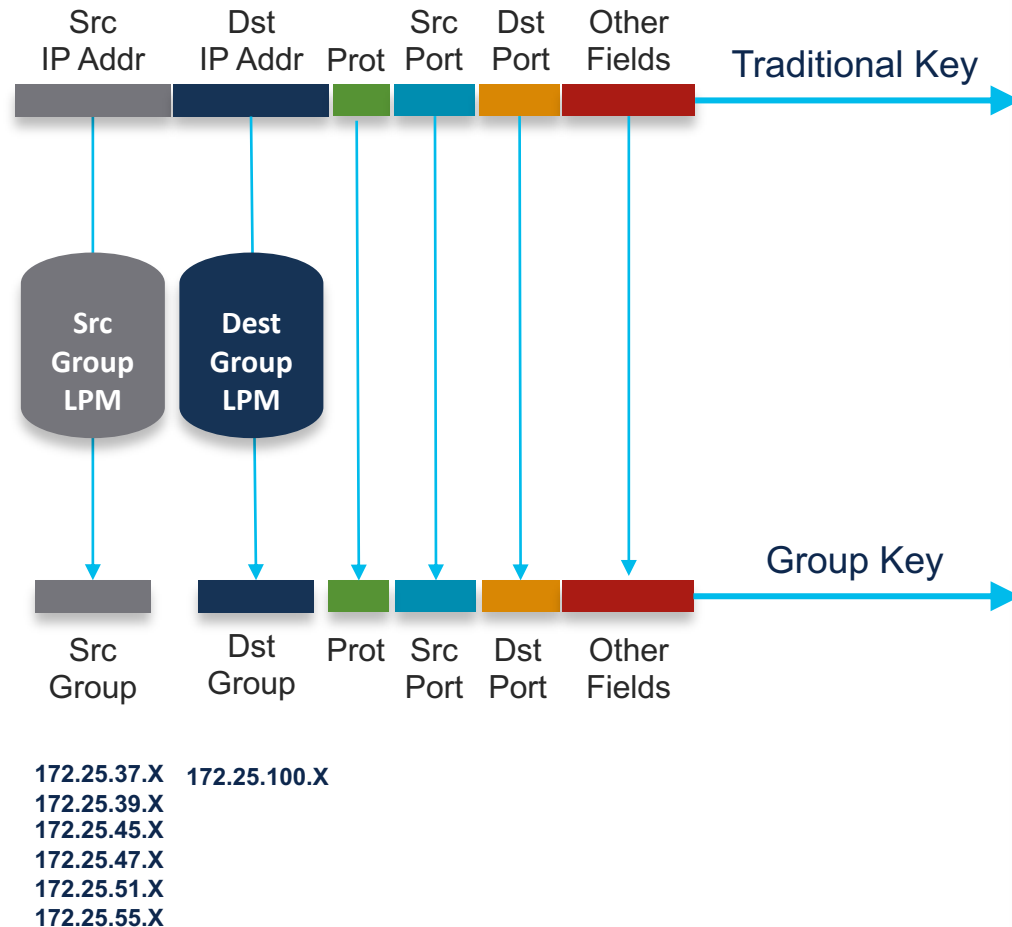
Object-Groups map IP/mask to Labels in CEM

- User defines IP/masks to simple OG name
- OGID labels are stored in Exact Match table

OGACL ACEs take minimal space in ACL TCAM

- Only the Permit/Deny ACEs in TCAM
- OGACLs with same ACEs can reuse entries

Traditional ACL vs Group-Based ACL



Traditional ACL: One TCAM entry per ACL entry

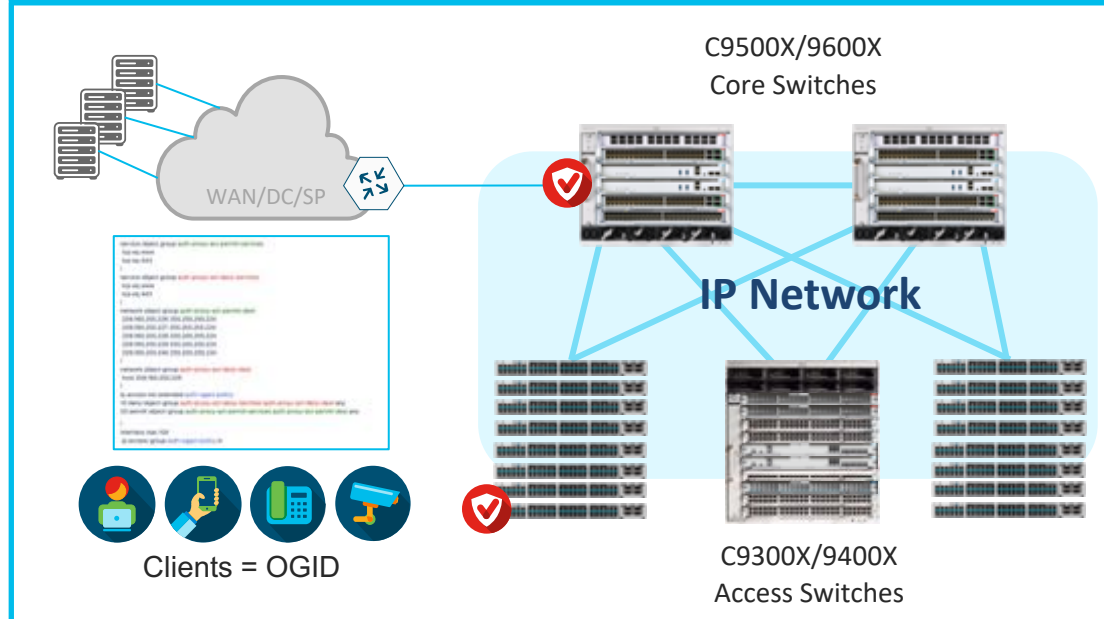
perrrmit udp 172.25.37.0/24 any 172.25.100.0/24 any
perrrmit udp 172.25.39.0/24 any 172.25.100.0/24 any
perrrmit udp 172.25.45.0/24 any 172.25.100.0/24 any
perrrmit udp 172.25.47.0/24 any 172.25.100.0/24 any
perrrmit udp 172.25.51.0/24 any 172.25.100.0/24 any
perrrmit udp 172.25.55.0/24 any 172.25.100.0/24 any
Free
Free

Object Group ACL: One TCAM entry per group-combo

perrrmit udp object-group G1 any object-group G2 any
Free
Free
Free
Free
Free
Free
Free

Why OGACL/SGACL in Campus Core?

Object-Group ACLs for IP



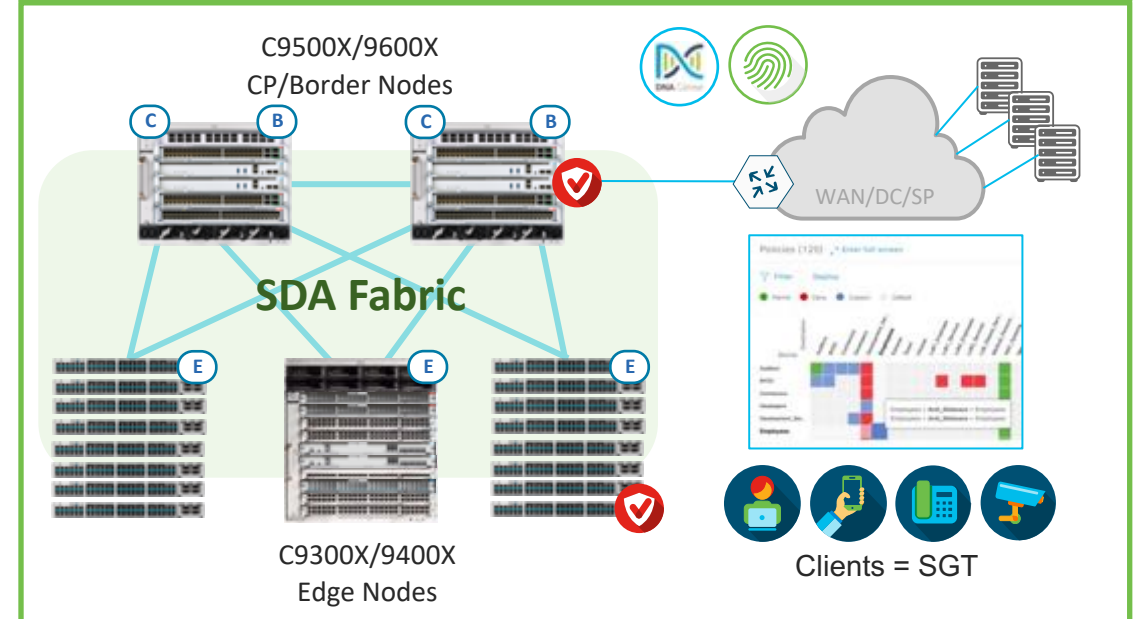
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OGACL ACEs take minimal space in ACL TCAM

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- OGACLs with same ACEs can reuse entries

Scalable-Groups for SDA



Scalable-Groups map IP/mask to Labels in CEM

- ISE/DNAC defines IP/masks to simple SG name
- SGT labels are stored in Exact Match table

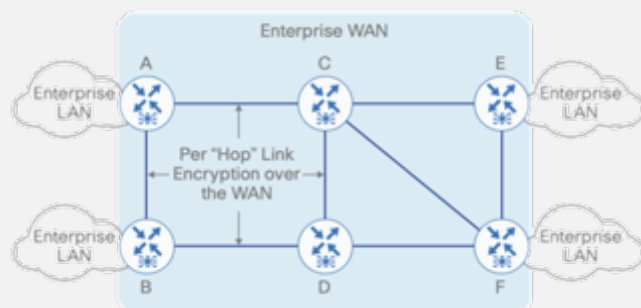
SGACL ACEs take minimal space in ACL TCAM

- Only the Permit/Deny ACEs in TCAM
- SGACLs with same ACEs can reuse entries

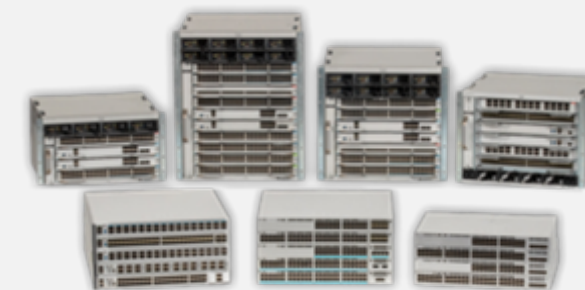
LAN & WAN MACsec overview

Enabled in hardware on Catalyst 9000 Switches

MACsec

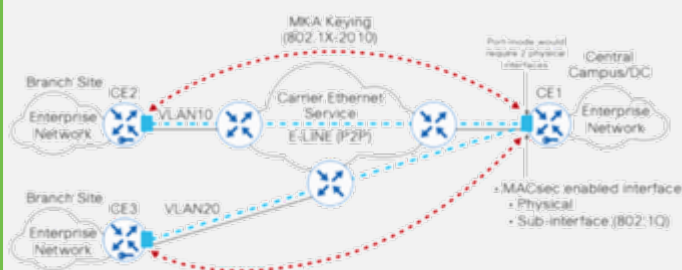


- **Hop-by-Hop encryption**
- Directly connected **Layer 2 links only**
 - 802.1ae
- Secure direct P2P links between Campus, MAN or DC
- 256/128-bit AES encryption



Supported on **all Catalyst® 9000** models
All ports and speeds simultaneously

WAN MACsec*



- **End-to-End encryption**, across Layer 2 Ethernet WAN service
- 802.1q ClearTag
- **Point-to-Point** or **Point-to-Multipoint**
- Secure Site-to-Site interconnect, DCI, storage replication
- 256/128-bit AES encryption



Catalyst 9600X



Catalyst 9500X

Supported on **Silicon One™** platforms*
All ports/speeds (up to 400G) simultaneously



Catalyst 9400X

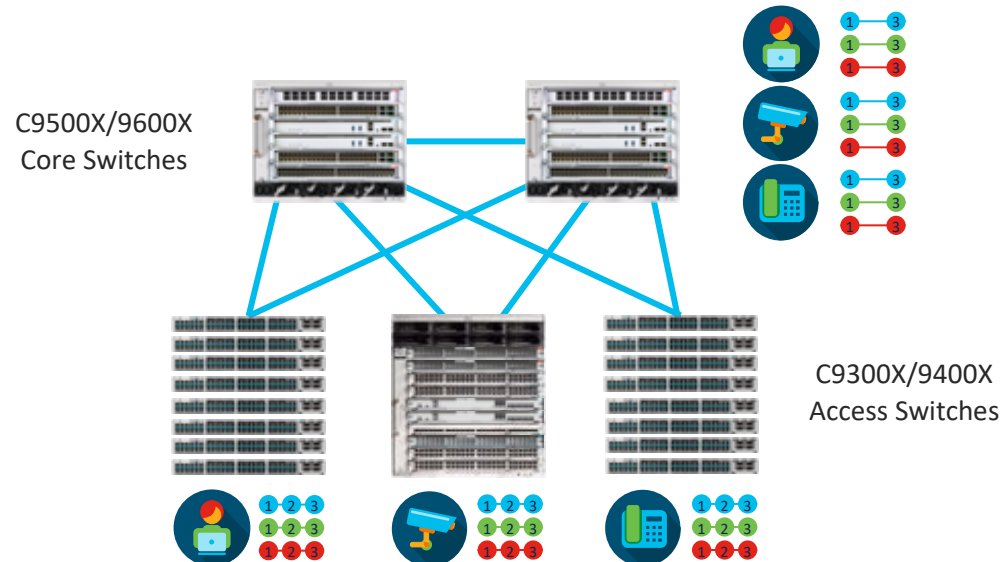


Catalyst 9300X

Roadmap for Catalyst 9300X & 9400X
Aggregate speed up to 100G

Why Sampled FNF in Campus Core?

ID @ Access – Monitor @ Core



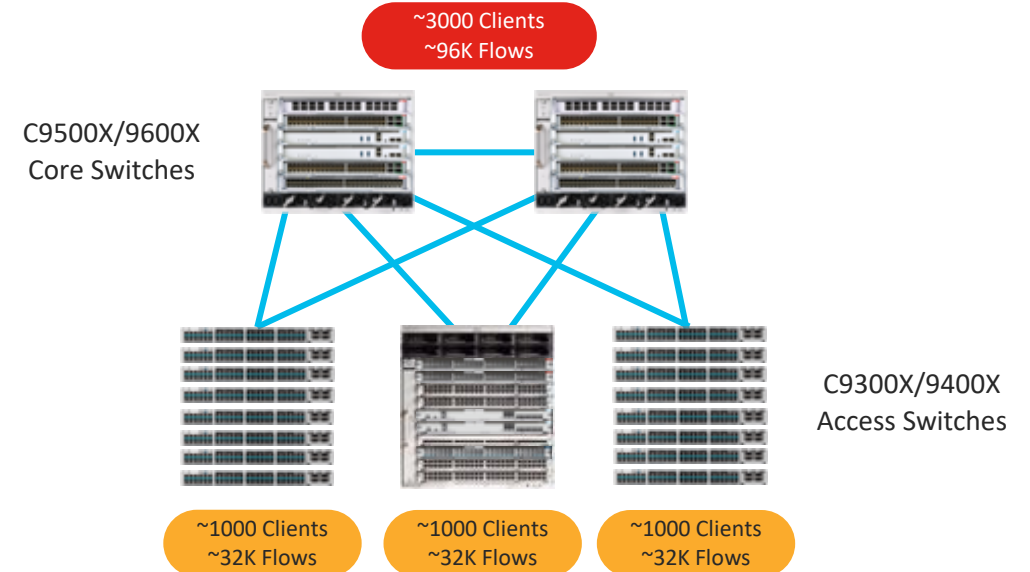
Detailed (1:1) flow identification at the Access

- Better to ID flows as they enter the network
- Full accounting of every client/flow (ETA/AVC)

Aggregate (1:1K) monitoring of flows at the Core

- Just need to monitor the overall network usage
- Adjust sample rates to balance scale & load

Campus-wide Scale



Low-Moderate scale at the Access

- Fewer number of connected clients/flows
- Average ~1K clients x ~32K flows per Access

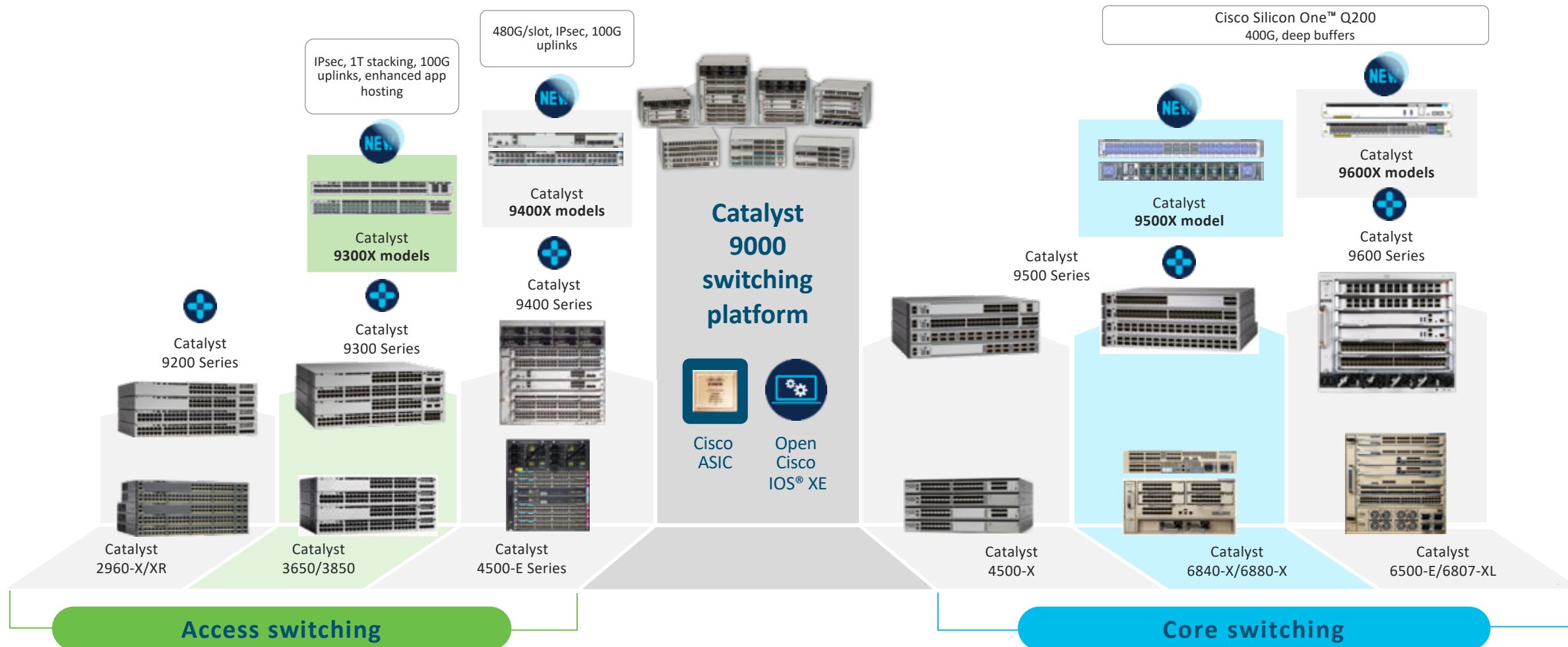
Medium-High scale at the Core

- Need to aggregate all clients/flows (# Access x 32K)
- Adjust cache aging to increase overall scale

Summary

Catalyst 9000X – Expanding industry leadership

Adding the “X factor” to the industry’s leading switching family



Fragen?



OUTLOOK Upcoming Virtual Espresso

- Blog:
<http://cs.co/vEspresso>
- Topics:
 - 23.03.2022: WiFi Innovations
 - 06.04.2022: Routing Innovations
 - 24.04.2022: DevNet Use Cases
 - 18.05.2022: Secure Network Analytics



dankä villmal
grazie mille
merci beaucoup
grazia fitg
thank you

